

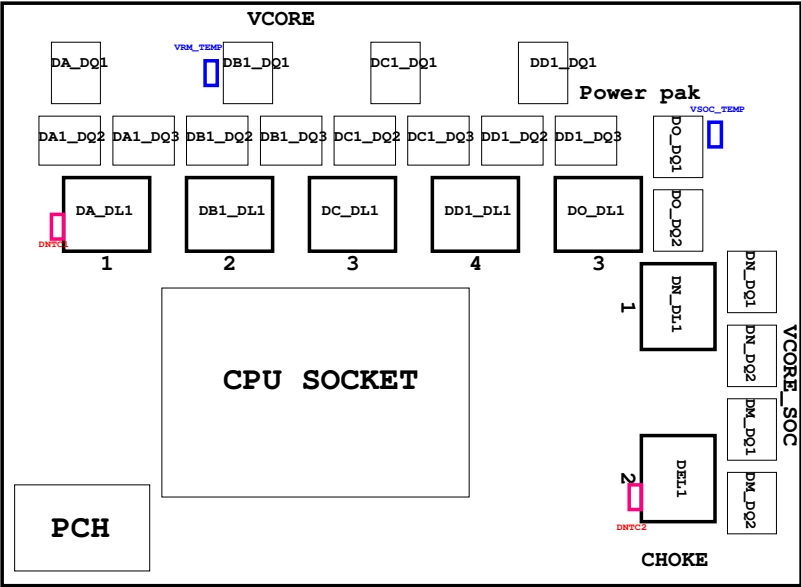
A520M S2H

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Model Name: A520M S2H

Component value change history

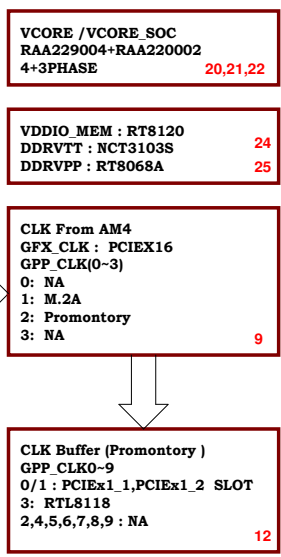
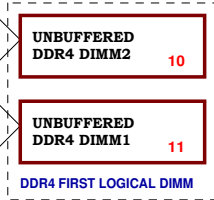
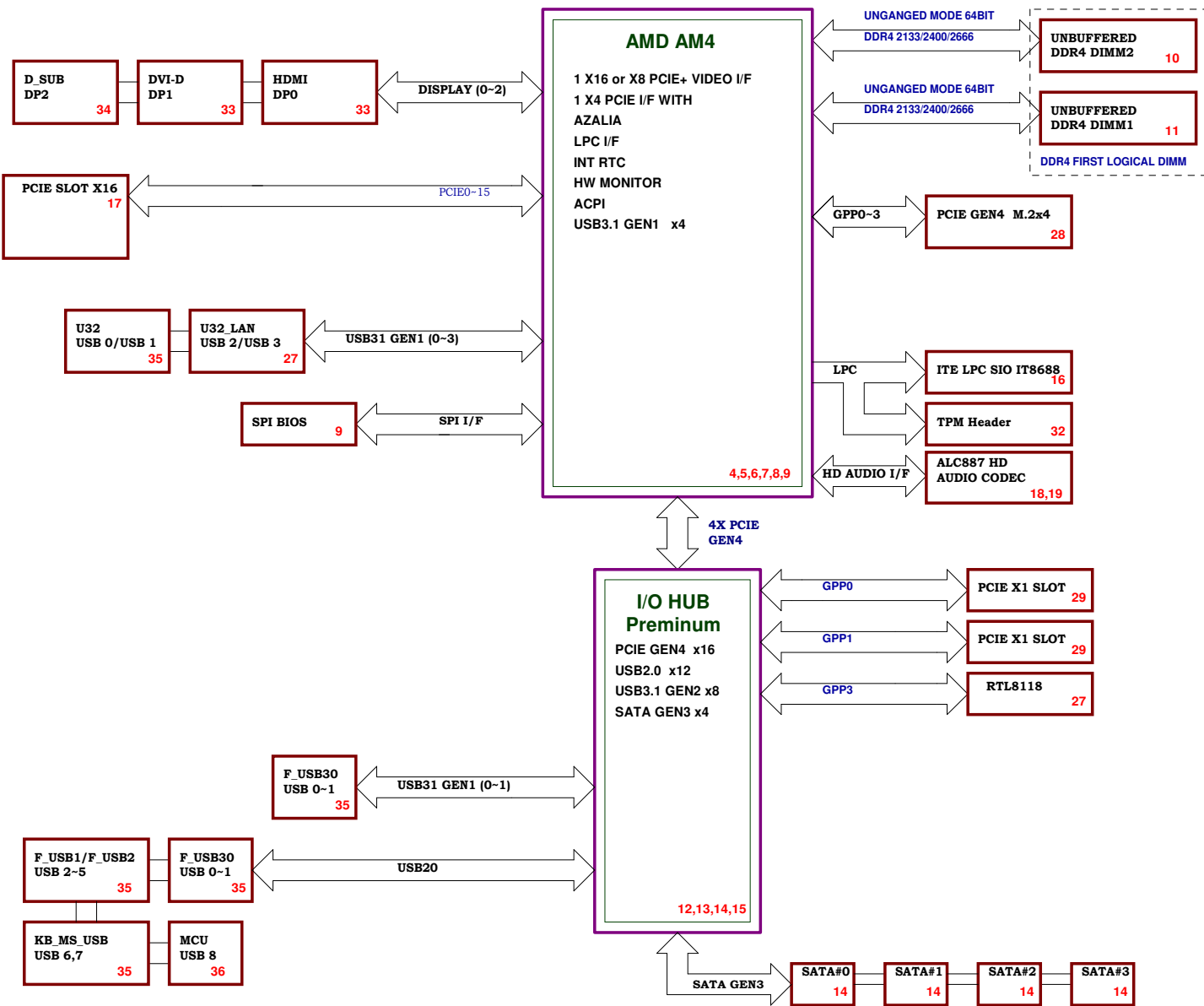
Version: 1.02

P-Code: U98126-0

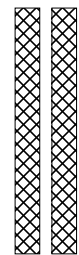
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Circuit or PCB layout change for next version

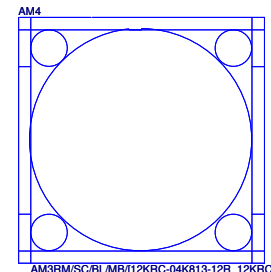
[illegible]



MEM CHA



- [10] MODT_A0[0..3] <=> MODT_A0[0..3]
- [10] MDA[0..63] <=> MDA[0..63]
- [10] MAAA[0..16] <=> MAAA[0..16]
- [10] DQSA[0..8] <=> DQSA[0..8]
- [10] -DQSA[0..8] <=> -DQSA[0..8]



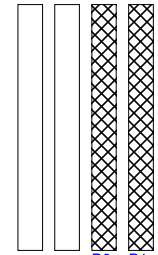
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Title: **APU DDR4**

Size: Custom Document Number: **A520M S2H** Rev: **1.02**

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MEM CHB

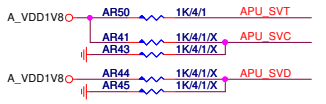
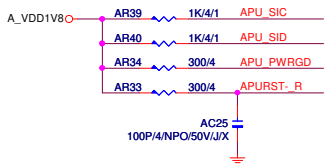


- [11] MB_CLKH2 <=> MB_CLKH2
- [11] MB_CLKL2 <=> MB_CLKL2
- [11] MB_CLKH3 <=> MB_CLKH3
- [11] MB_CLKL3 <=> MB_CLKL3

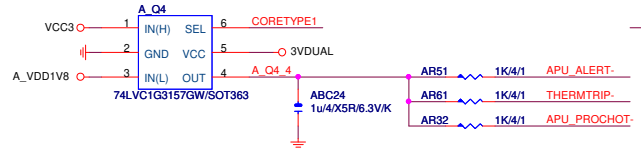
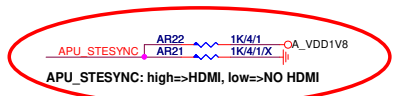
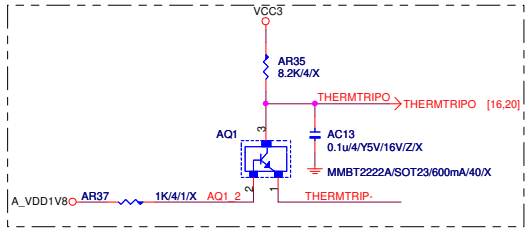
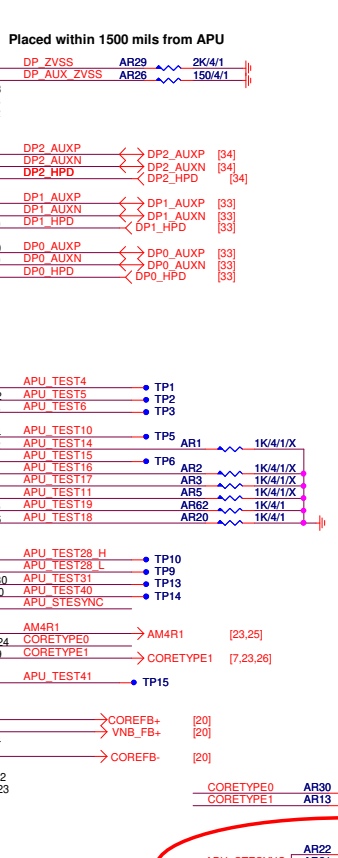
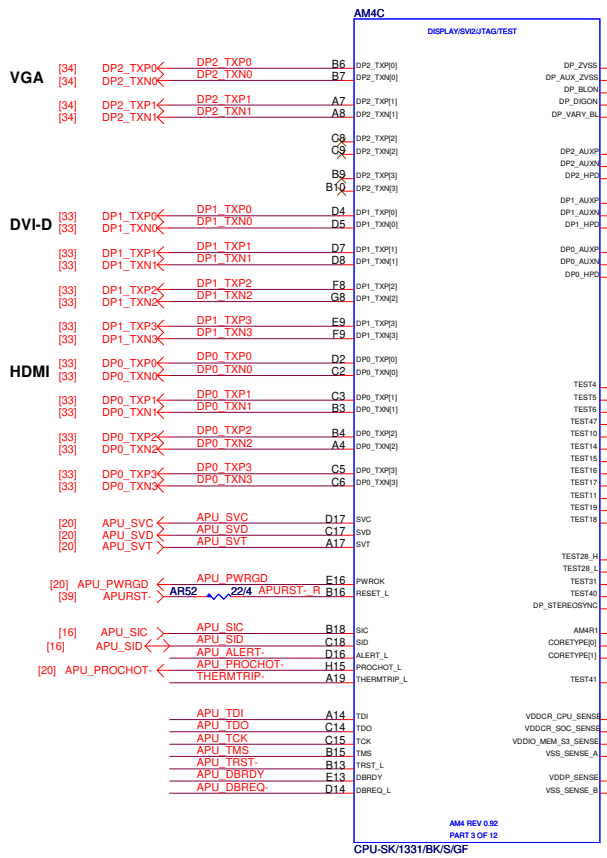
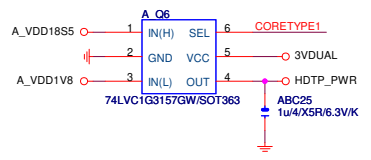
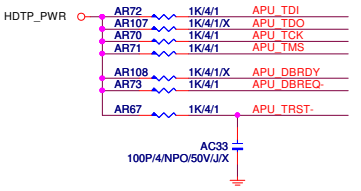
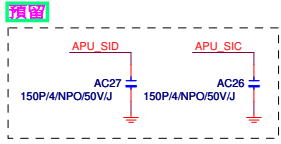
- [11] MODT_B[0..3] <=> MODT_B[0..3]
- [11] MDB[0..63] <=> MDB[0..63]
- [11] MAAB[0..16] <=> MAAB[0..16]
- [11] DQSB[0..8] <=> DQSB[0..8]
- [11] -DQSB[0..8] <=> -DQSB[0..8]

A0 A1

B0 B1



SVC	SVD	Boot voltage
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



CORETYPE 1	CORETYPE 0	Family / Model Numbers	AM4 APU TYPE
0 BR	0	Family 15 h / Models 60 h-6 Fh	TYPE 0
0 ST	1	Reserved	TYPE 1
1 ZP	0	Family 17 h / Models 00 h-0 Fh	TYPE 2
1 RV	1	Family 17 h / Models 10 h-1 Fh	TYPE 3

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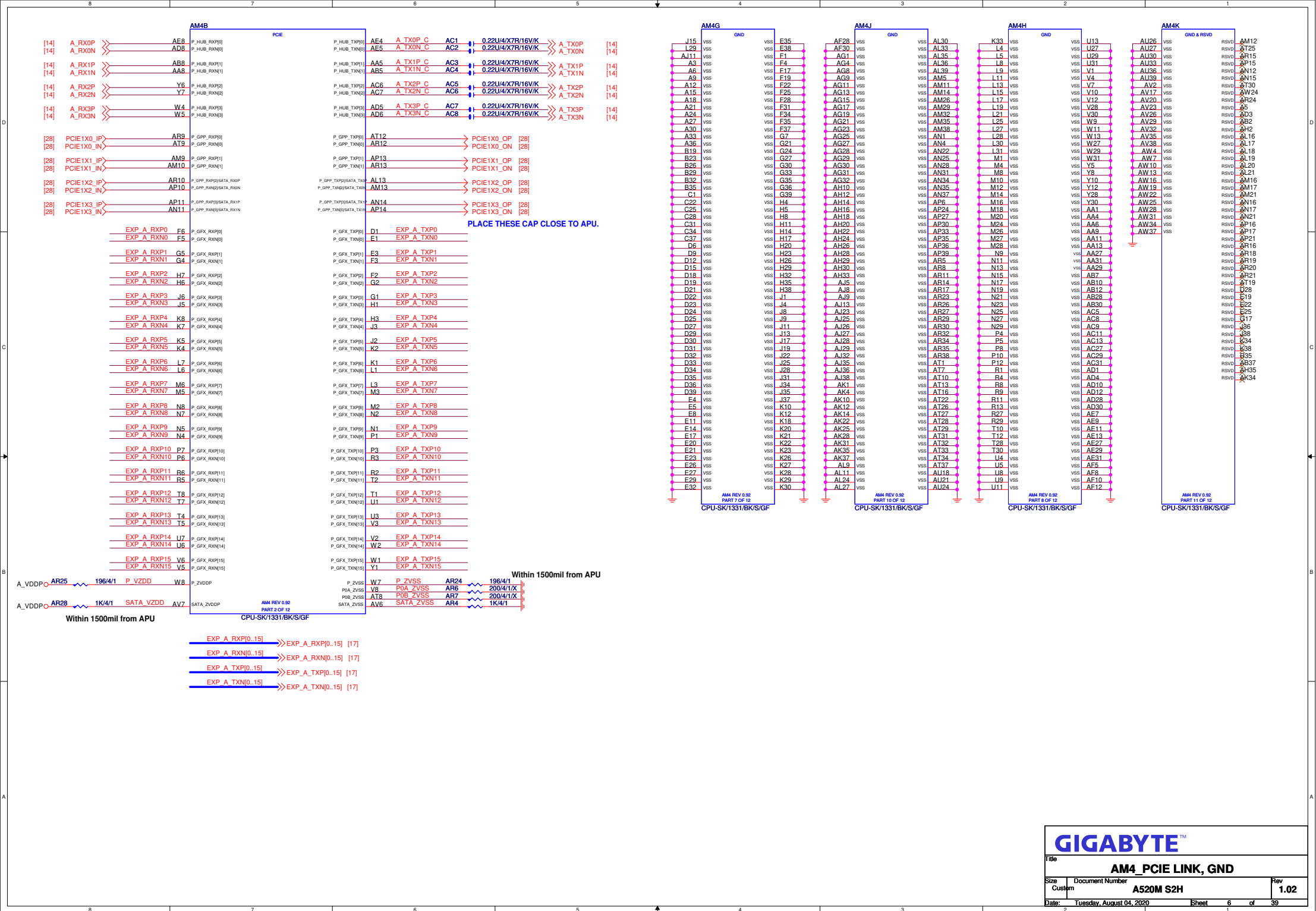
CPU CONTROL

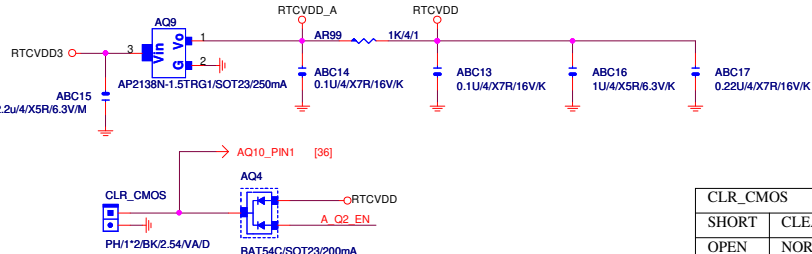
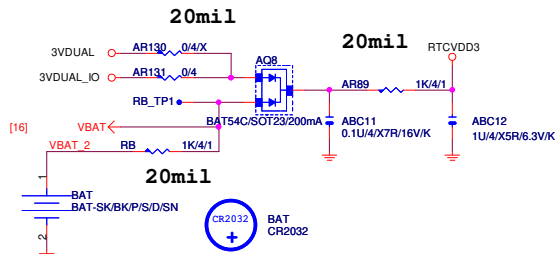
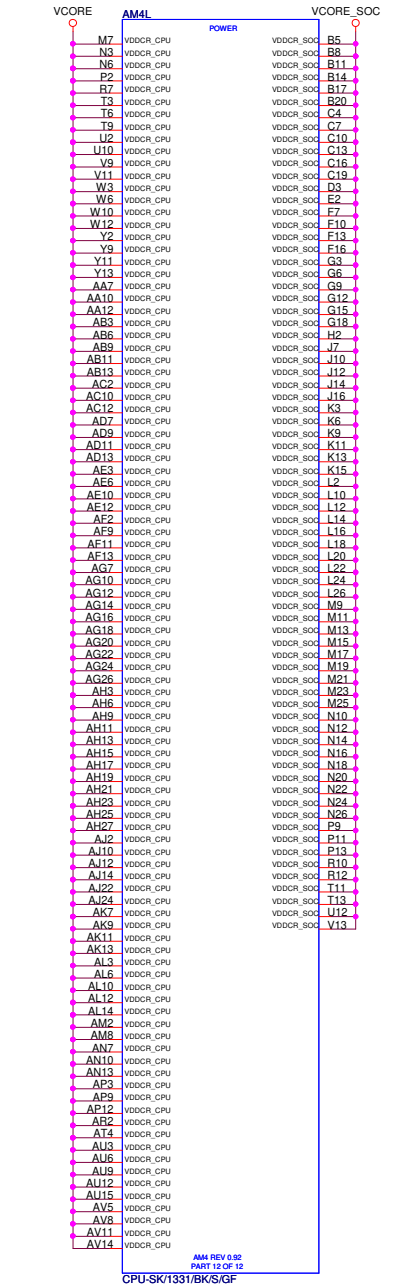
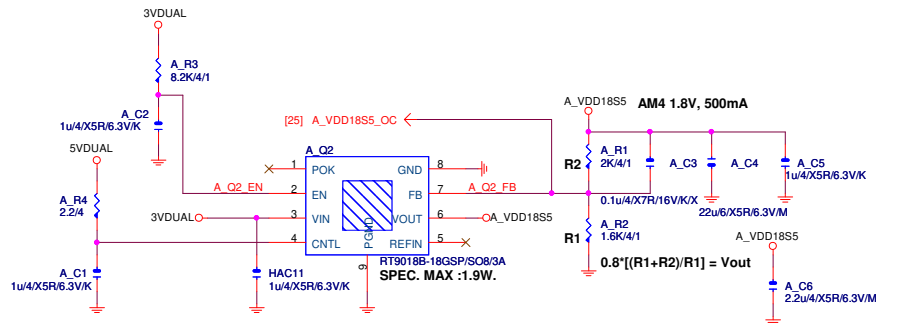
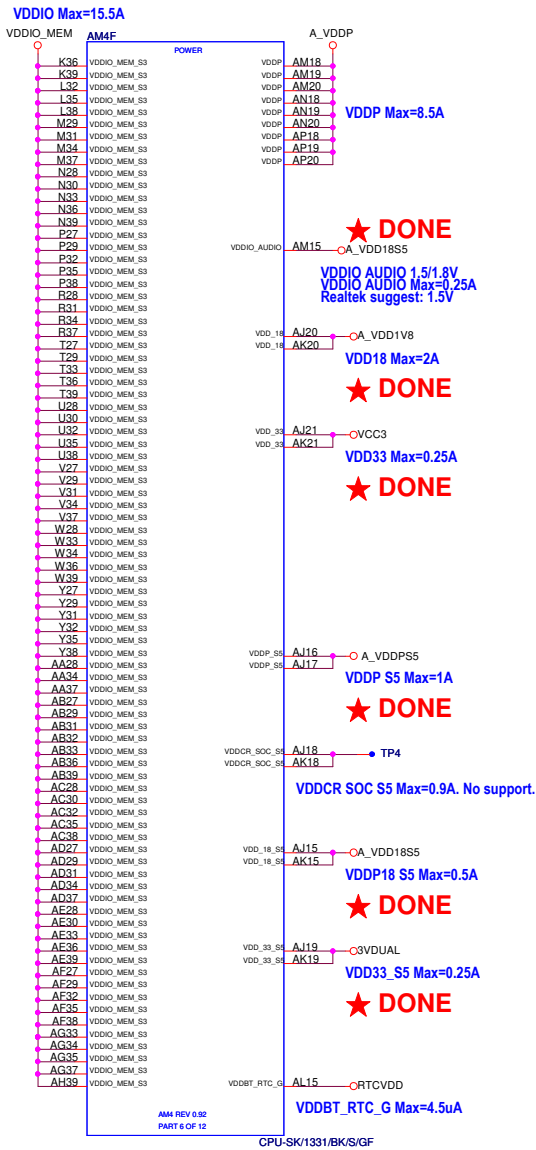
Document Number
A520M S2H

Rev
1.02

Date: Tuesday, August 04, 2020

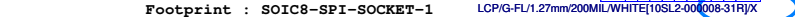
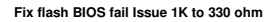
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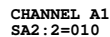


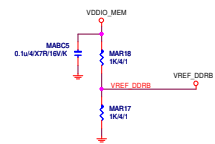
CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL
NOT ADD ICT FOR RTCVDD PIN	

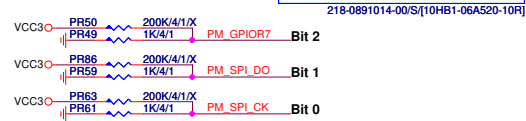
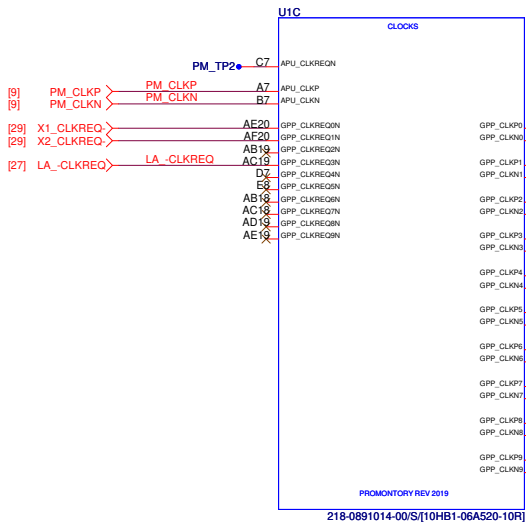
GIGABYTE™			
Title CPU POWER & GND			
Size	Document Number	Rev	
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Date: Tuesday, August 04, 2020 Sheet 9 of 39







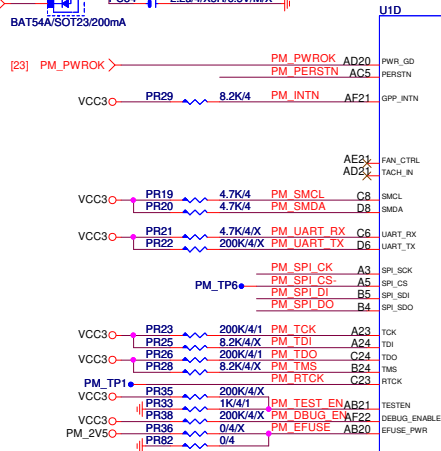
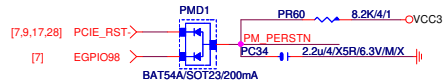
Bit 2	Bit 1	Bit 0	GPP Group 0 (Lanes 3:0)
0	0	0	4 PCIe x1
0	0	1	2 PCIe x1 + 1 PCIe x2
0	1	0	1 PCIe x2 + 2 PCIe x1
0	1	1	1 PCIe x2 + 1 PCIe x2
1	1	1	1 PCIe x4
Others: Reserved			



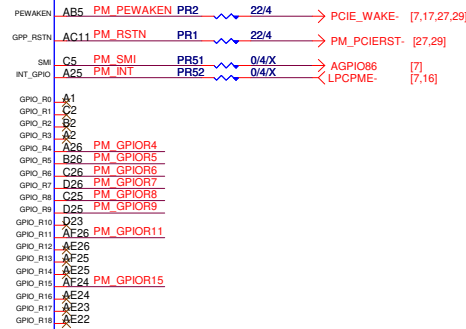
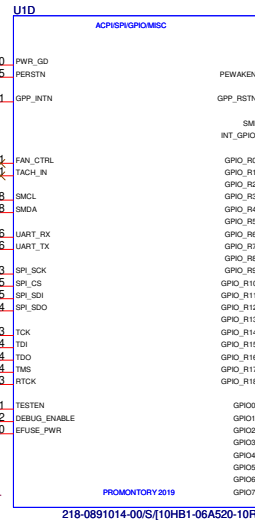
Bit 2	Bit 1	Bit 0	GPP Group 1 (Lanes 7:4)
0	0	0	4 PCIe x1
0	0	1	2 PCIe x1 + 1 PCIe x2
0	1	0	1 PCIe x2 + 2 PCIe x1
0	1	1	1 PCIe x2 + 1 PCIe x2
1	1	1	1 PCIe x4
Others: Reserved			



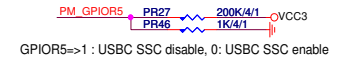
GPP Group 2 (Lan 8:9)=>1: PCIe x2, 0: 2 PCIe x1



PR71 1K/4/1 PM_DEBUG_EN
PR79 1K/4/X PM_TCK
PR80 1K/4/X PM_TDO
TESTEN=>1:Test Mode, 0:Function mode.
DEBUG=>1:Debug Mode, 0:Function mode.

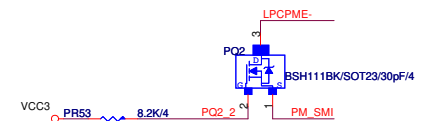
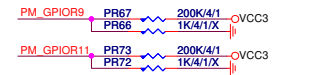


PM_GPIOR4 PR10 200K/4/1 VCC3
PR12 1K/4/1 X
GPIOR4 1: GPP clock source from APU_CLKP/N;
0: GPP clock source from Crystal.

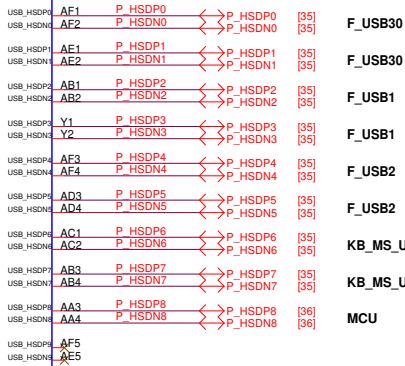
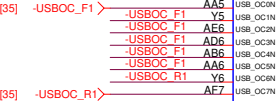


GPIOR5=>1: USB SSC disable, 0: USB SSC enable

GPIOR6=>1: SATA SSC disable, 0: SATA SSC enable



USB port power control 9:0
(VCC3). Output.



F_USB30

F_USB30

F_USB1

F_USB1

F_USB2

F_USB2

KB_MS_USB

KB_MS_USB

MCU

USB 3.1 Gen 2

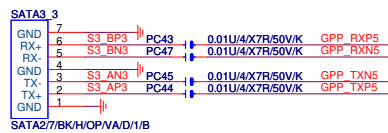
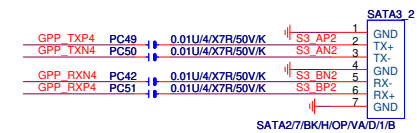
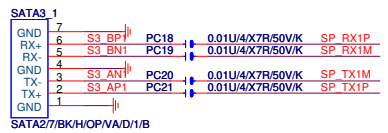
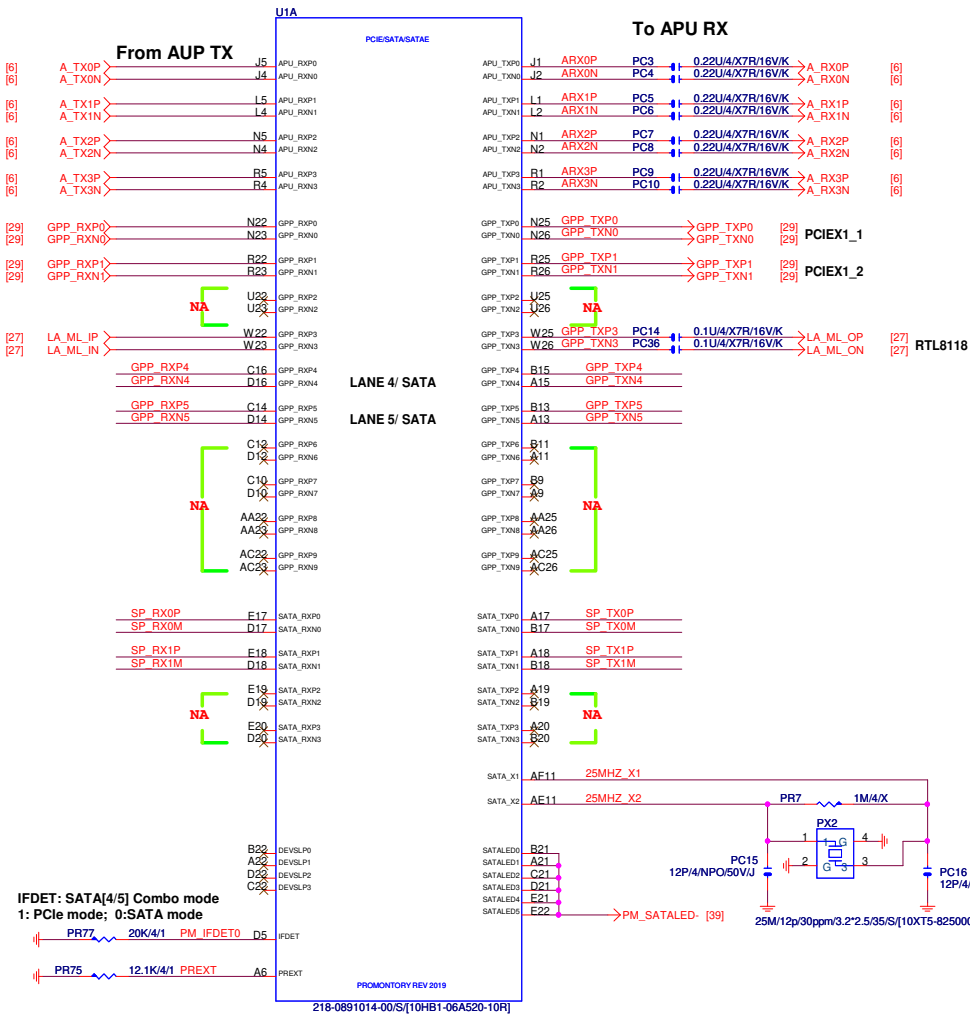


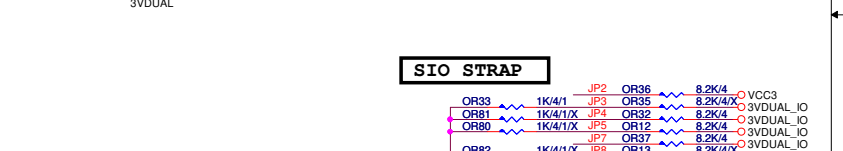
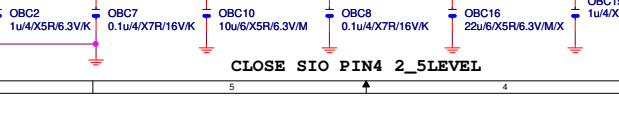
F_USB30

F_USB30

PROMONTORY REV 2019
218-0891014-00/S[10HB1-06A520-10R]

USB32G2	USB20	USB_OC
0	0	0
1	1	1
USB32G1		
0	2	2
1	3	3
	4	4
	5	5
	6	6
	7	7
	8	7
	9	7

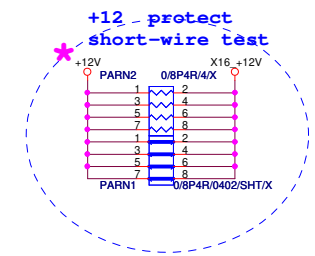
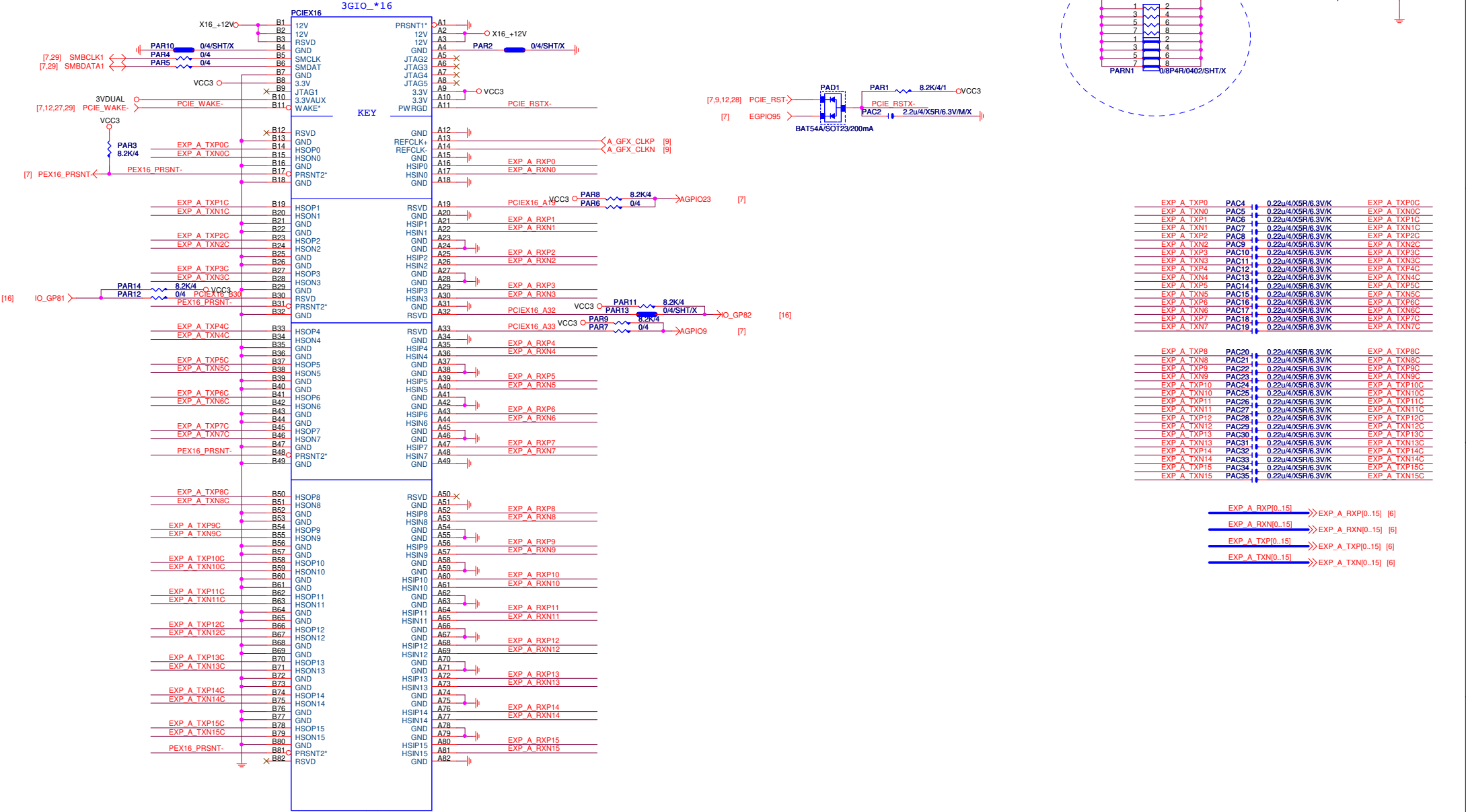




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size	Document Number	Rev	Customer
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2		1	

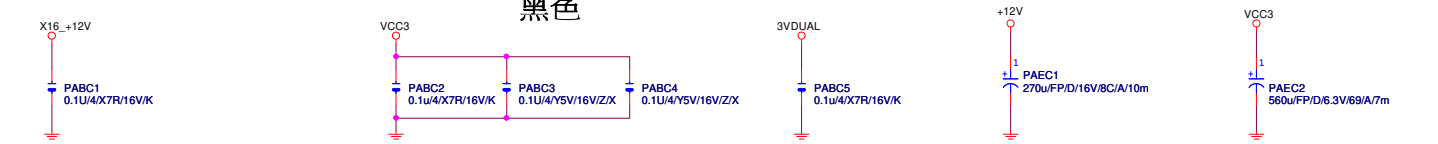
★ Footprint : PCIESLOT-164P

3GIO_*16



EXP A TXP0	PAC4	0.22u4/X5R6.3V/K	EXP A TXP0C
EXP A TXN0	PAC5	0.22u4/X5R6.3V/K	EXP A TXN0C
EXP A TXP1	PAC6	0.22u4/X5R6.3V/K	EXP A TXP1C
EXP A TXN1	PAC7	0.22u4/X5R6.3V/K	EXP A TXN1C
EXP A TXP2	PAC8	0.22u4/X5R6.3V/K	EXP A TXP2C
EXP A TXN2	PAC9	0.22u4/X5R6.3V/K	EXP A TXN2C
EXP A TXP3	PAC10	0.22u4/X5R6.3V/K	EXP A TXP3C
EXP A TXN3	PAC11	0.22u4/X5R6.3V/K	EXP A TXN3C
EXP A TXP4	PAC12	0.22u4/X5R6.3V/K	EXP A TXP4C
EXP A TXN4	PAC13	0.22u4/X5R6.3V/K	EXP A TXN4C
EXP A TXP5	PAC14	0.22u4/X5R6.3V/K	EXP A TXP5C
EXP A TXN5	PAC15	0.22u4/X5R6.3V/K	EXP A TXN5C
EXP A TXP6	PAC16	0.22u4/X5R6.3V/K	EXP A TXP6C
EXP A TXN6	PAC17	0.22u4/X5R6.3V/K	EXP A TXN6C
EXP A TXP7	PAC18	0.22u4/X5R6.3V/K	EXP A TXP7C
EXP A TXN7	PAC19	0.22u4/X5R6.3V/K	EXP A TXN7C
EXP A TXP8	PAC20	0.22u4/X5R6.3V/K	EXP A TXP8C
EXP A TXN8	PAC21	0.22u4/X5R6.3V/K	EXP A TXN8C
EXP A TXP9	PAC22	0.22u4/X5R6.3V/K	EXP A TXP9C
EXP A TXN9	PAC23	0.22u4/X5R6.3V/K	EXP A TXN9C
EXP A TXP10	PAC24	0.22u4/X5R6.3V/K	EXP A TXP10C
EXP A TXN10	PAC25	0.22u4/X5R6.3V/K	EXP A TXN10C
EXP A TXP11	PAC26	0.22u4/X5R6.3V/K	EXP A TXP11C
EXP A TXN11	PAC27	0.22u4/X5R6.3V/K	EXP A TXN11C
EXP A TXP12	PAC28	0.22u4/X5R6.3V/K	EXP A TXP12C
EXP A TXN12	PAC29	0.22u4/X5R6.3V/K	EXP A TXN12C
EXP A TXP13	PAC30	0.22u4/X5R6.3V/K	EXP A TXP13C
EXP A TXN13	PAC31	0.22u4/X5R6.3V/K	EXP A TXN13C
EXP A TXP14	PAC32	0.22u4/X5R6.3V/K	EXP A TXP14C
EXP A TXN14	PAC33	0.22u4/X5R6.3V/K	EXP A TXN14C
EXP A TXP15	PAC34	0.22u4/X5R6.3V/K	EXP A TXP15C
EXP A TXN15	PAC35	0.22u4/X5R6.3V/K	EXP A TXN15C

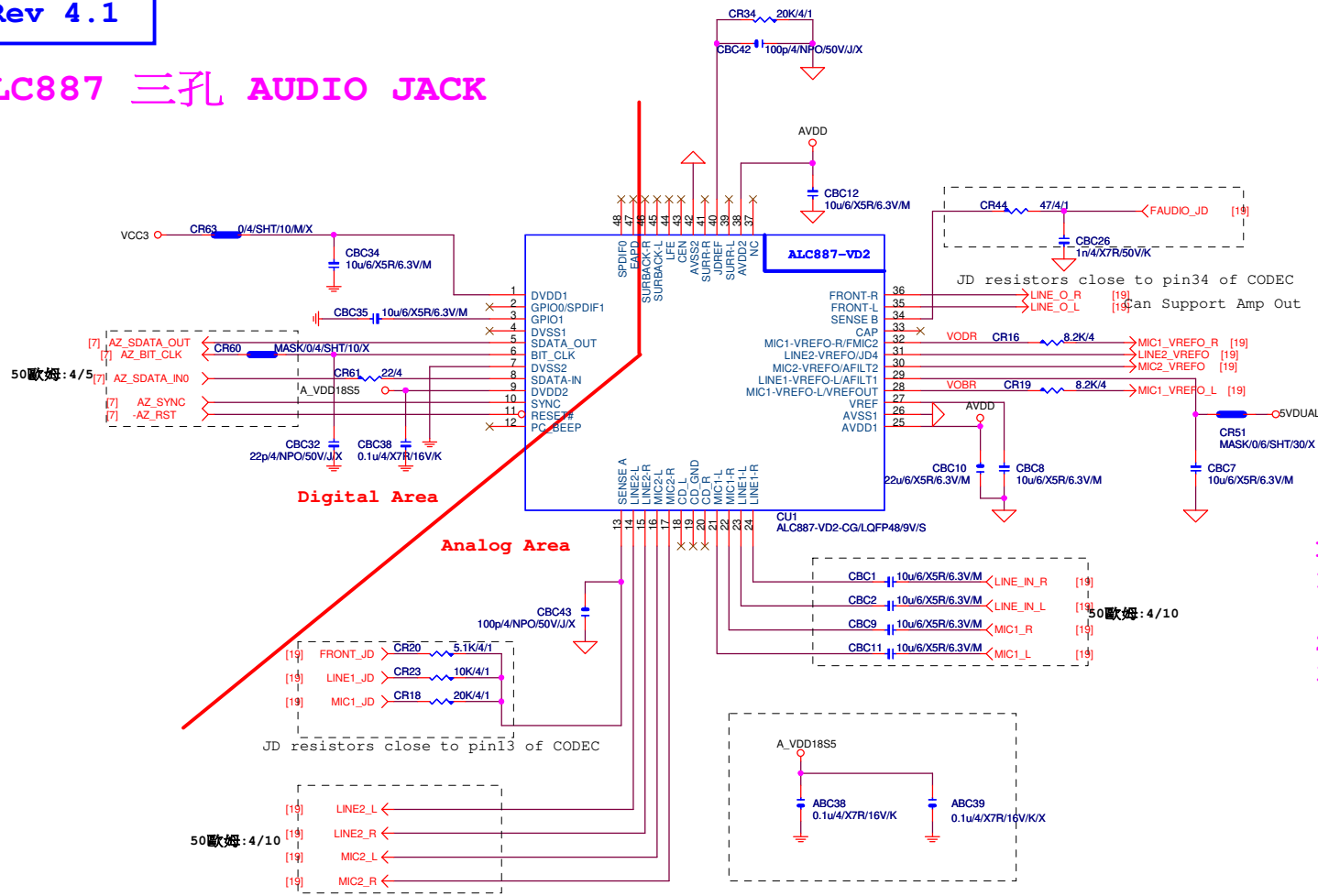
EXP A RXP[0..15] >> EXP_A_RXP[0..15] [6]
EXP A RXN[0..15] >> EXP_A_RXN[0..15] [6]
EXP A TXP[0..15] >> EXP_A_TXP[0..15] [6]
EXP A TXN[0..15] >> EXP_A_TXN[0..15] [6]



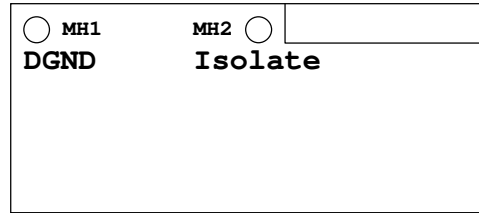
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Title PCI EXPRESS X 16		
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ALC887 三孔 AUDIO JACK

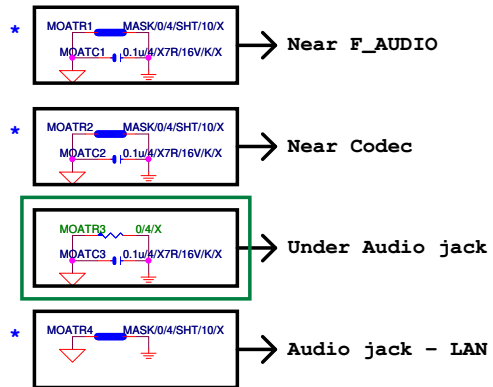


LAYOUT注意:螺絲孔下GND方式
1. MH1空間夠,下DGND
空間不夠,才改為Isolate
2. MH2一律改為Isolate
3. Codec下方,第二層必須參考GND



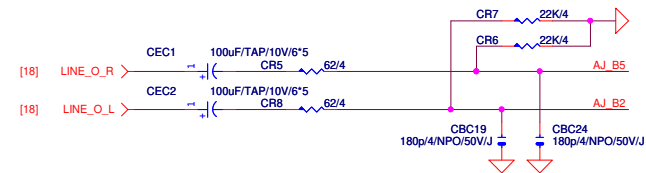
BOM OPTION : 1. Chemicon音效電容
2. 金屬外罩 Reserve (LAYOUT上件與否,依照各Model spec)
3. LED Reserve (上件與否和LED顏色,依照各Model spec)

Rev 4.1

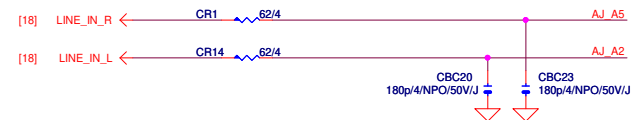


*量産前,MOATR1/MOATR2/MOATR40ohm改short pad

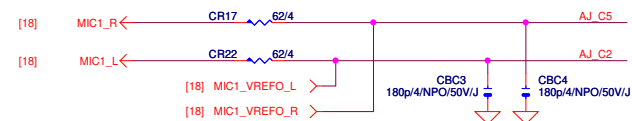
LINE-OUT



LINE-IN



MIC-IN

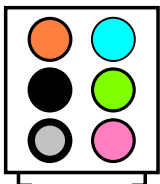


SURROUND

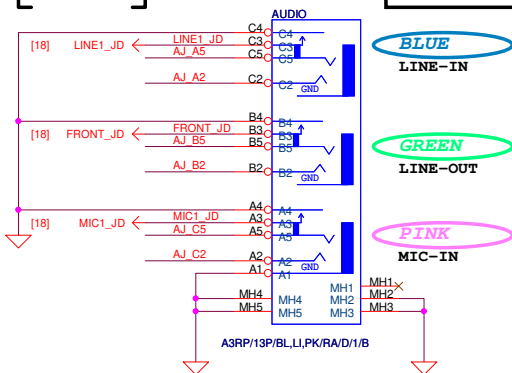
CEN/LFE

SURR BACK

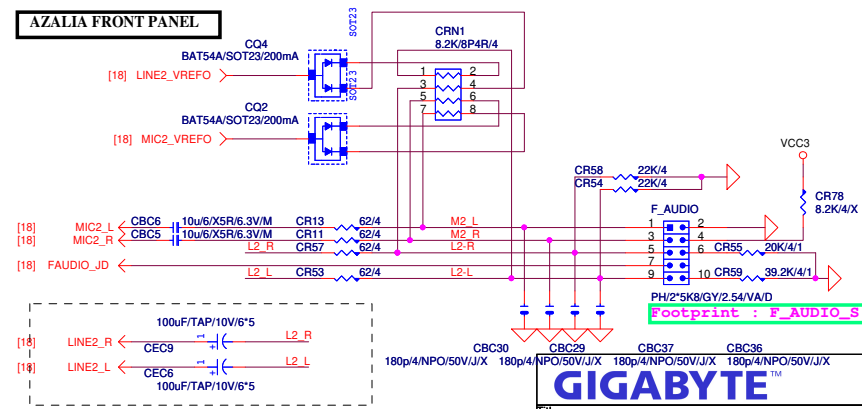
AZALIA JACK



AZALIA JACK

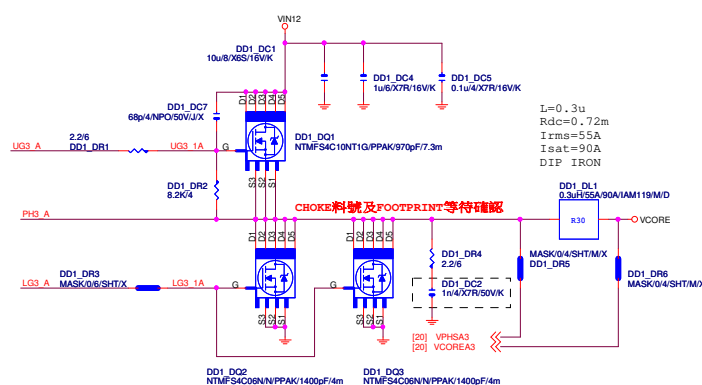
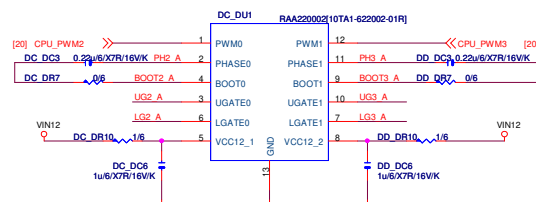
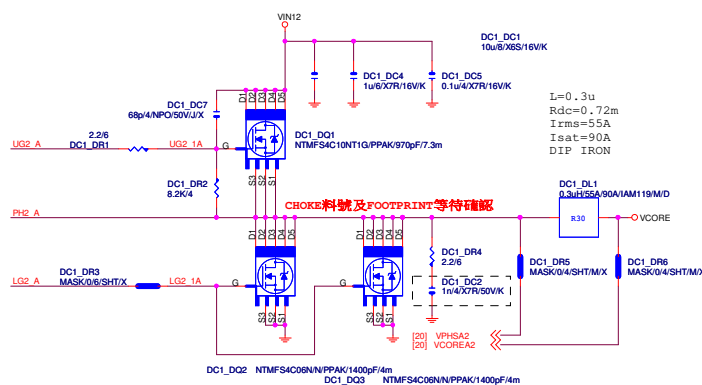


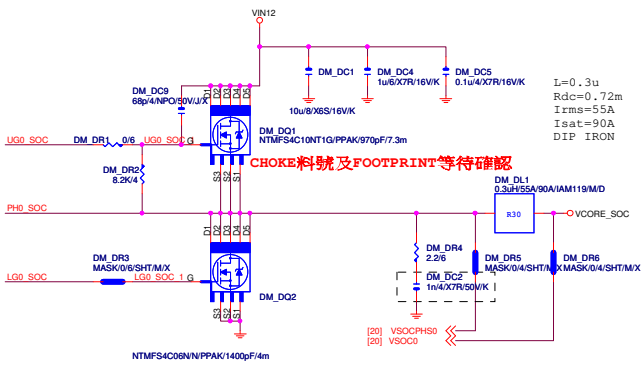
AZALIA FRONT PANEL



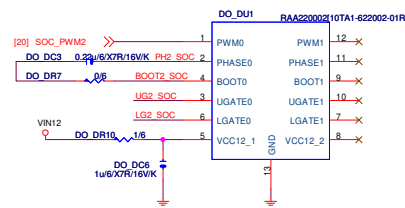
GIGABYTE

Title			
AUDIO JACK			
Size	Document Number		Rev
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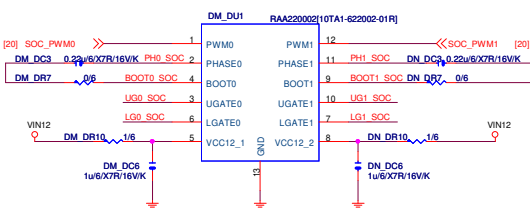




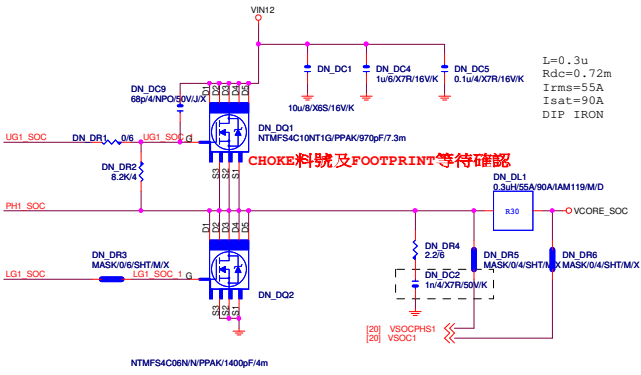
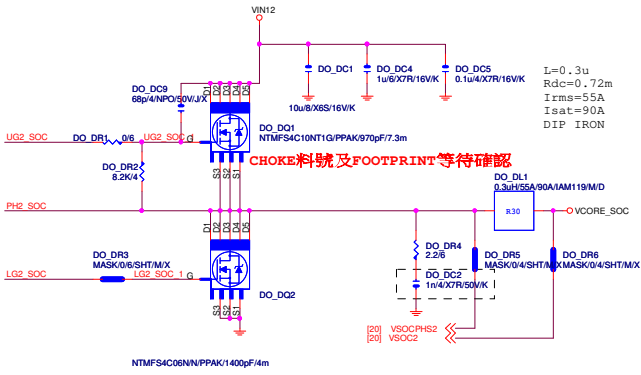
CHOKES料號及FOOTPRINT等待確認

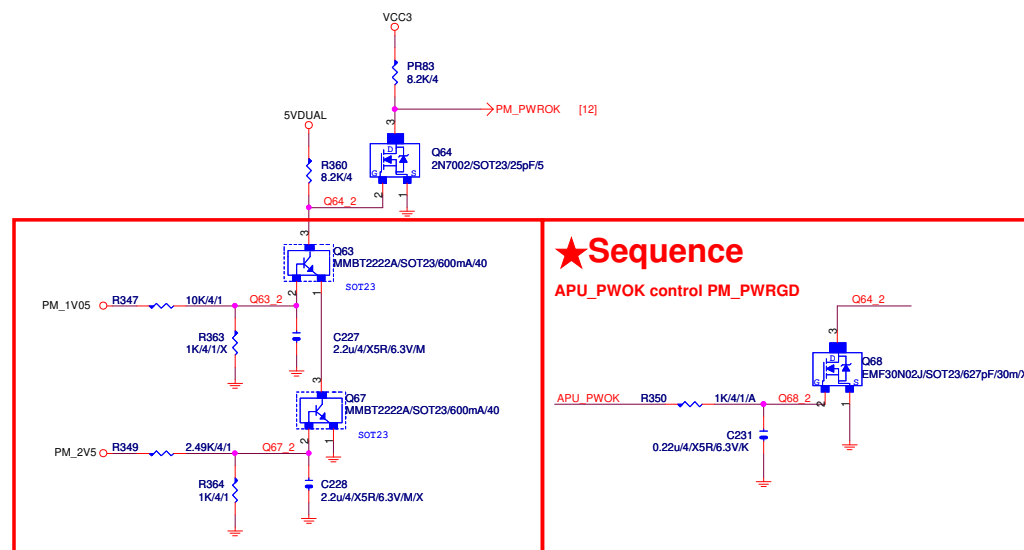
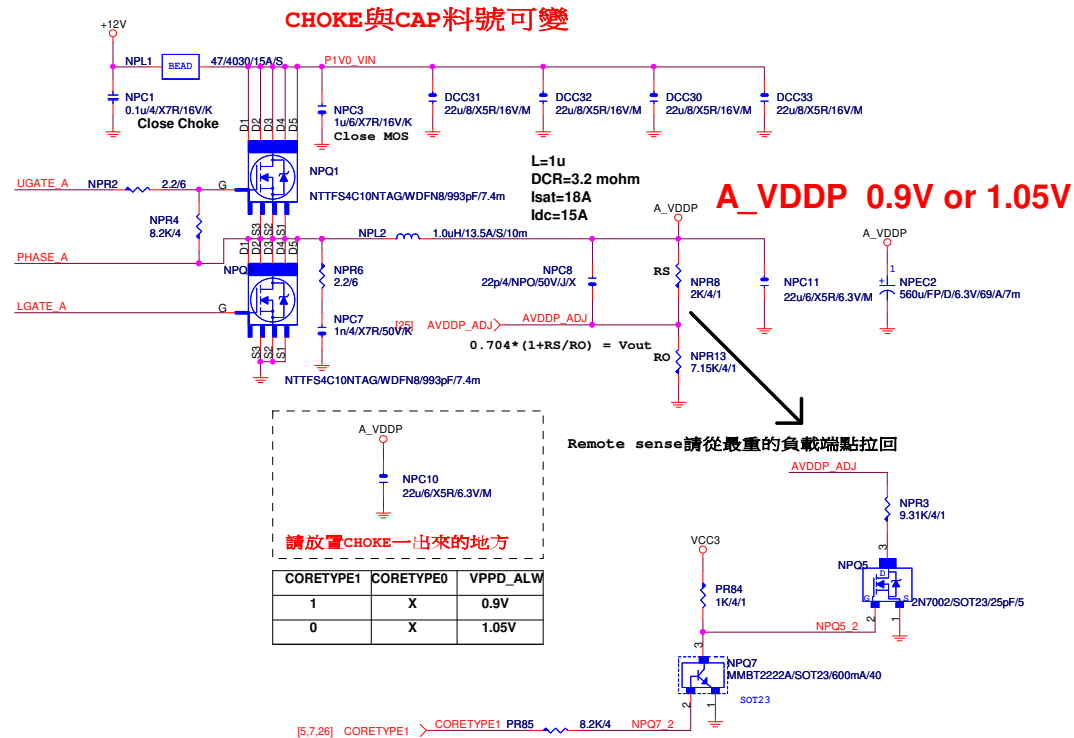
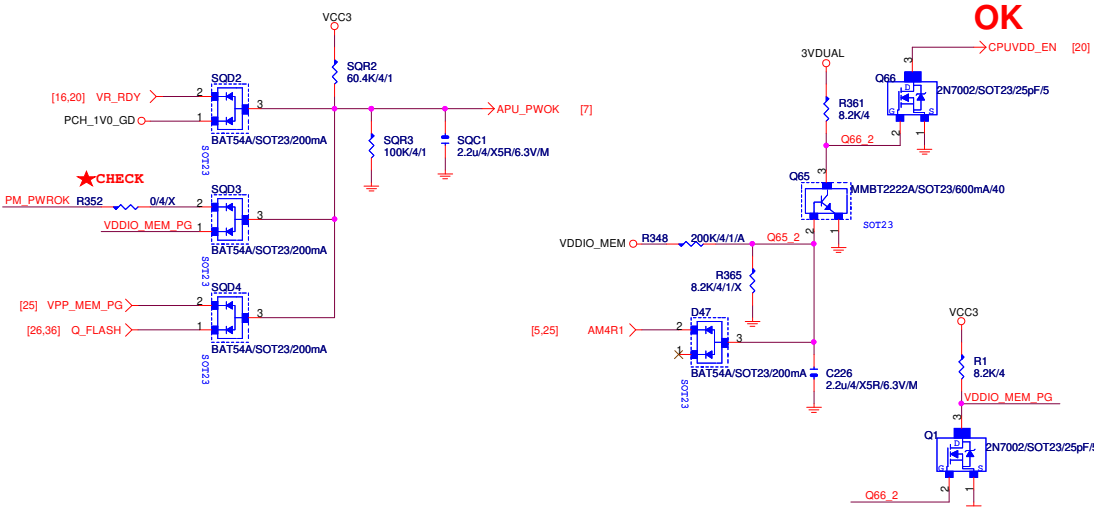


CHOKES料號及FOOTPRINT等待確認

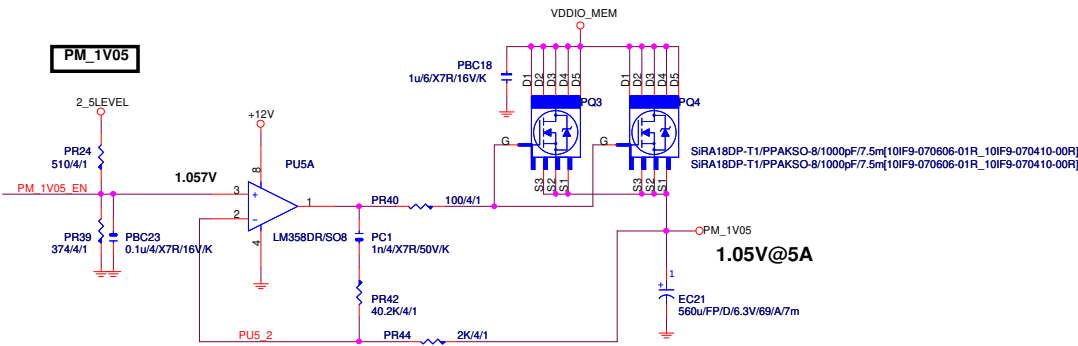


CHOKES料號及FOOTPRINT等待確認

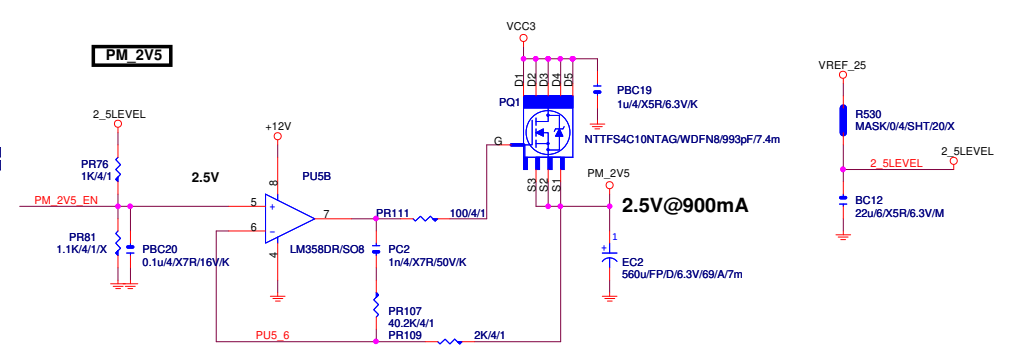




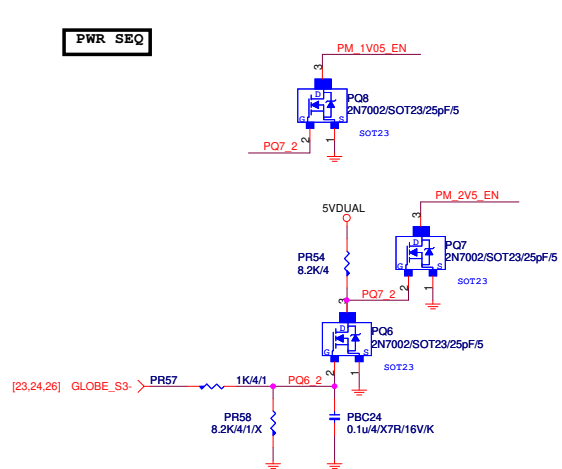
PM_1V05



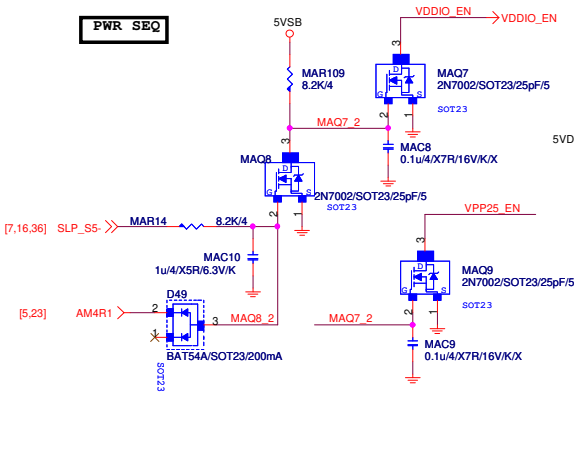
PM_2V5



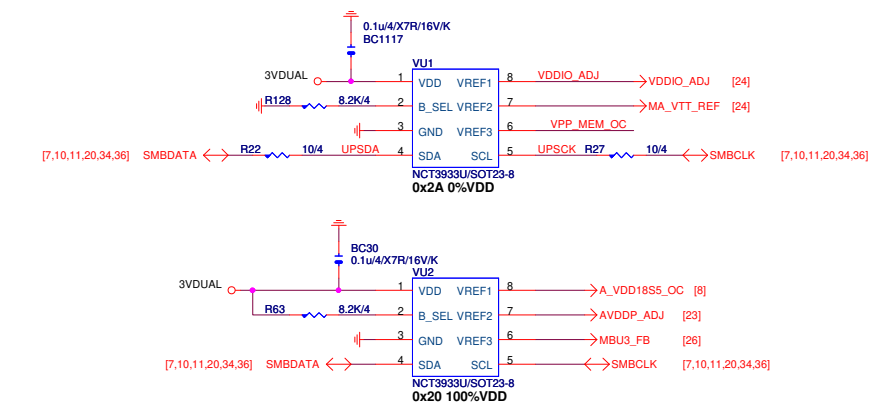
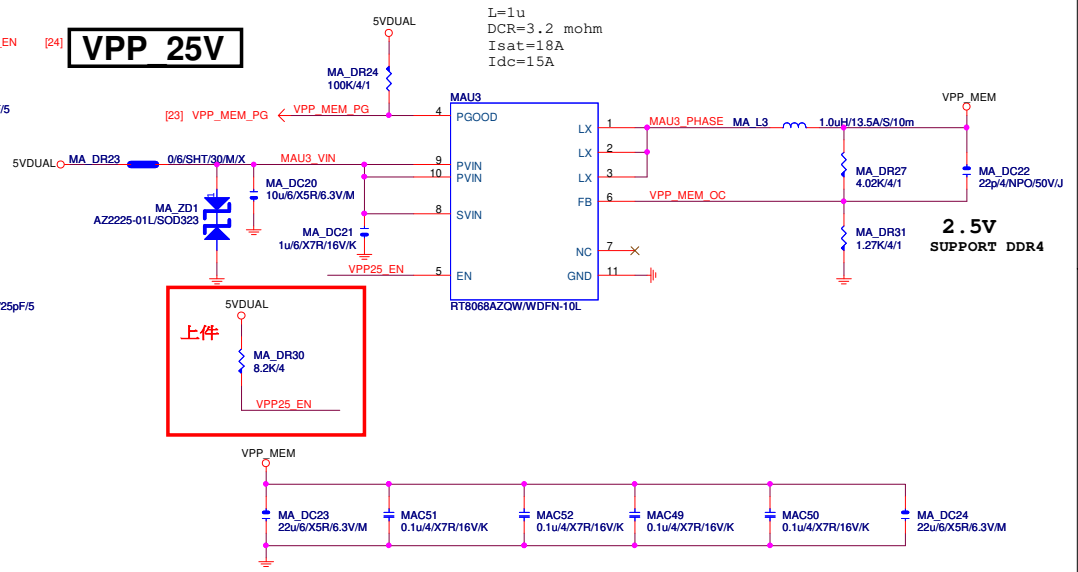
PWR_SEQ



PWR_SEQ



VPP 25V



Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (kΩ)	open	3.9	3	2.2	1.3	10
R2 (kΩ)	10	1.3	2.2	3	3.9	open
ADD_SEL Voltage (% of VCC)	0	25	42	58	75	100

Table1. Recommended Slave Address Setting

Title

PM POWER

Size Custom

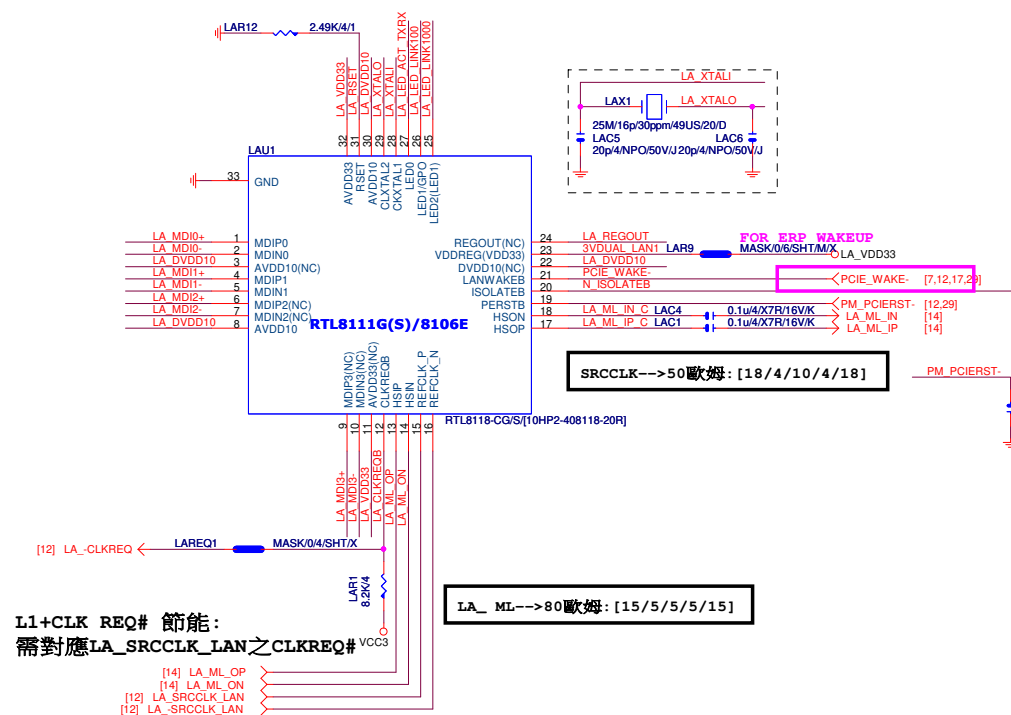
Document Number A520M S2H

Date: Tuesday, August 04, 2020

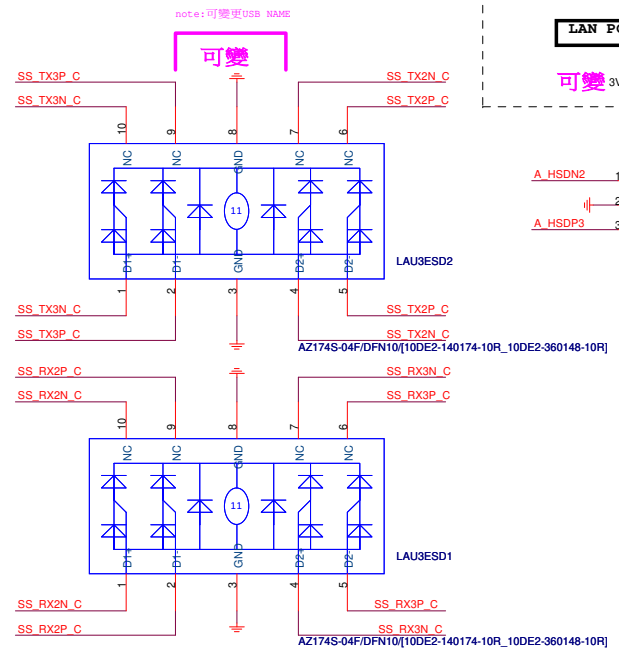
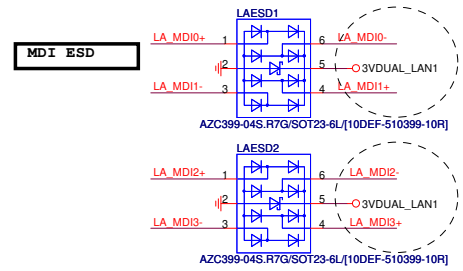
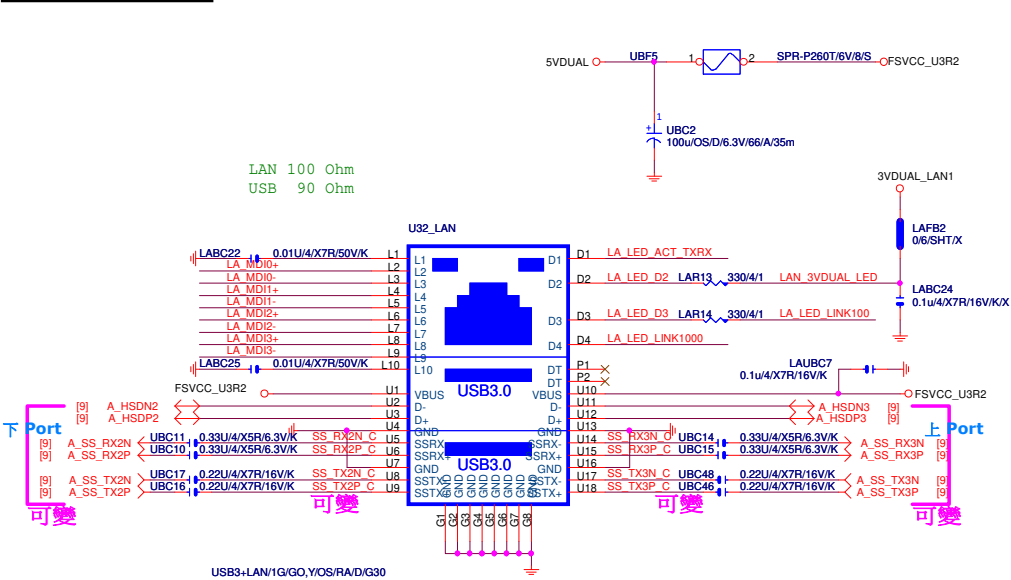
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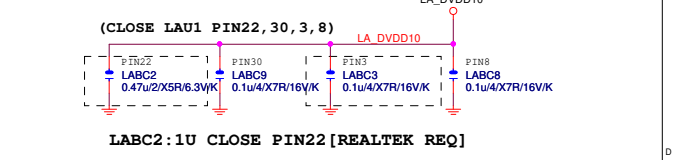
LAN:RTL8118 R2.03



USB_LAN CONNECTOR note:可變更USB NAME



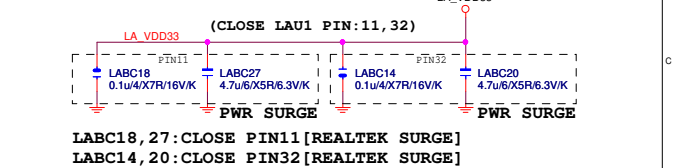
LAN POWER



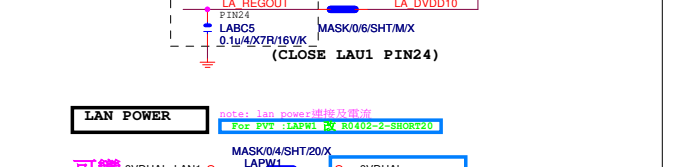
LAN POWER



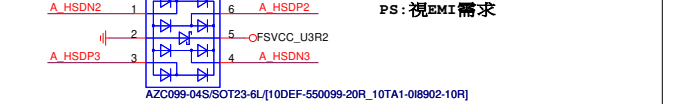
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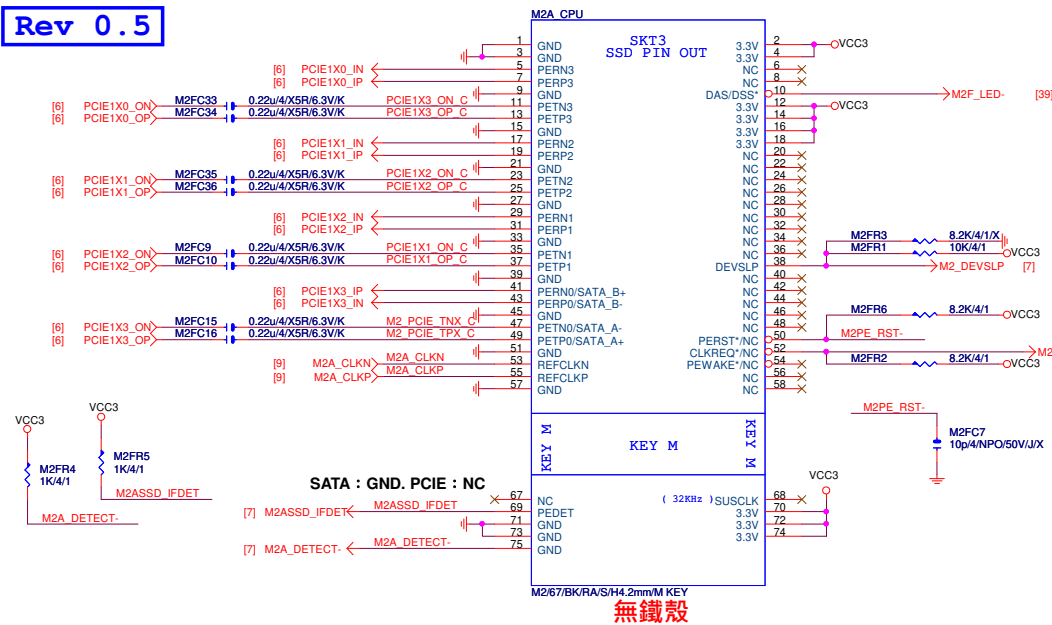
LAN POWER



LAN POWER

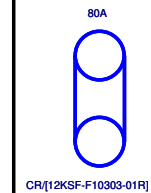


Rev 0.5



Footprint : NGFF-M-75P-8CM-09MM-SMD

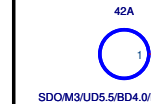
DIP螺柱



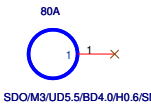
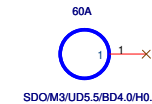
80A



SMD螺柱



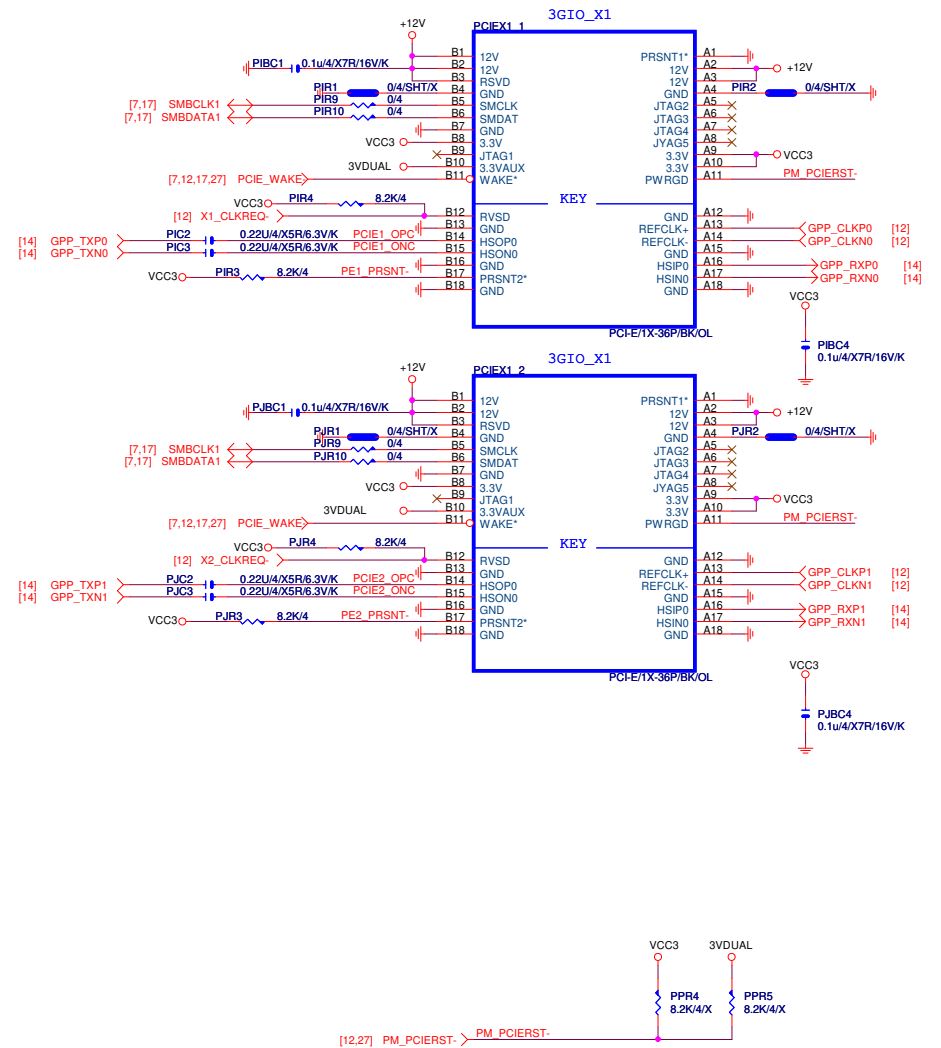
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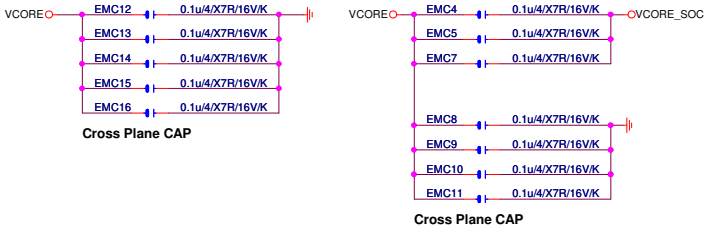
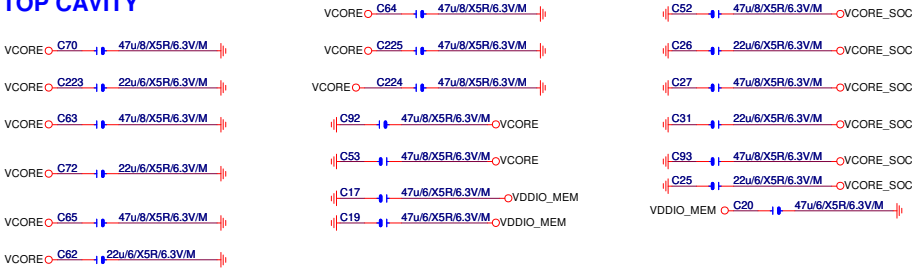
★ Footprint : HOLE_C236D165-A

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Title			U.2, M.2 SOCKET
Size			Custom
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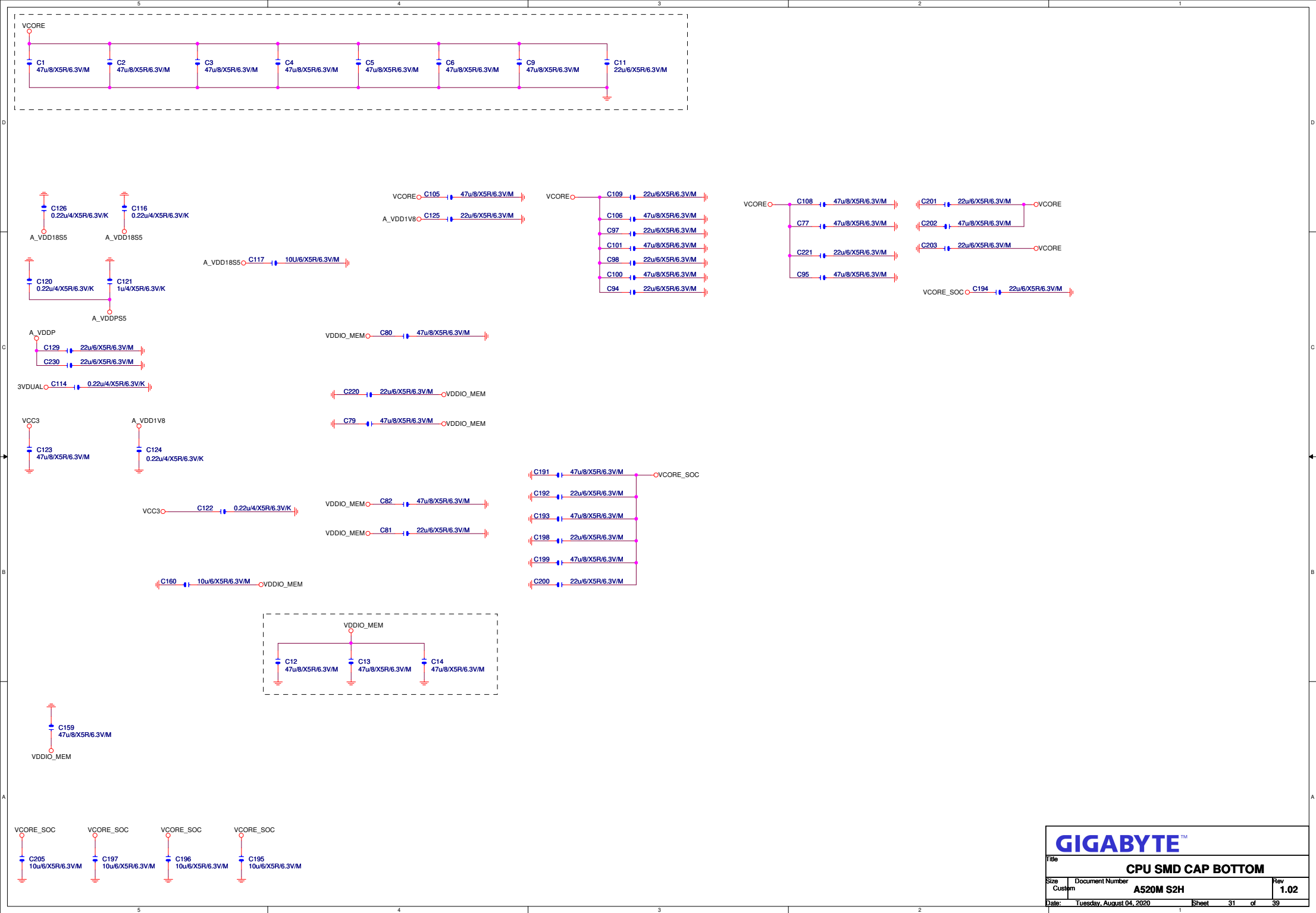
CPU TOP CAVITY

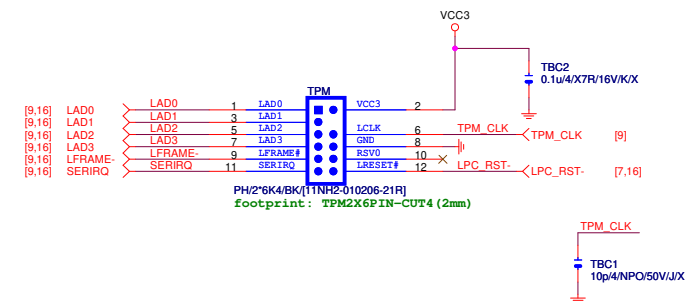


裝甲HEATSINK 分成五大部份

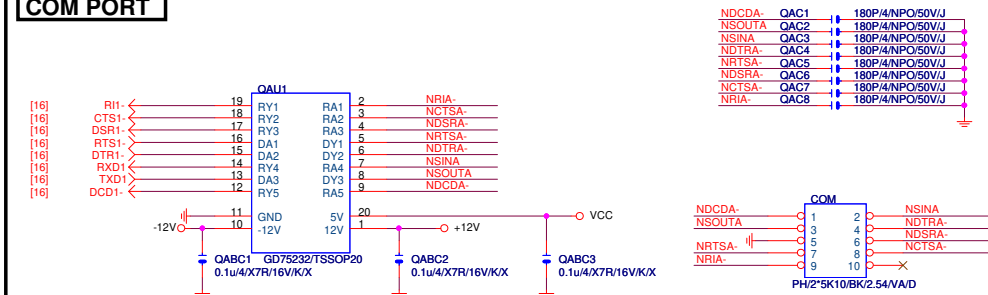


- * PCB顏色 : 咖啡黑
- * 文字面 : 灰色
- * 圖騰 : 同B450M S2H

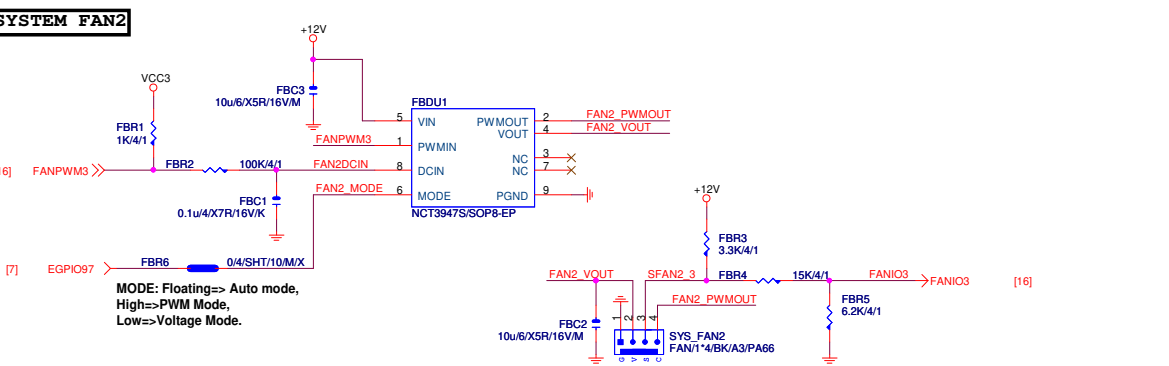
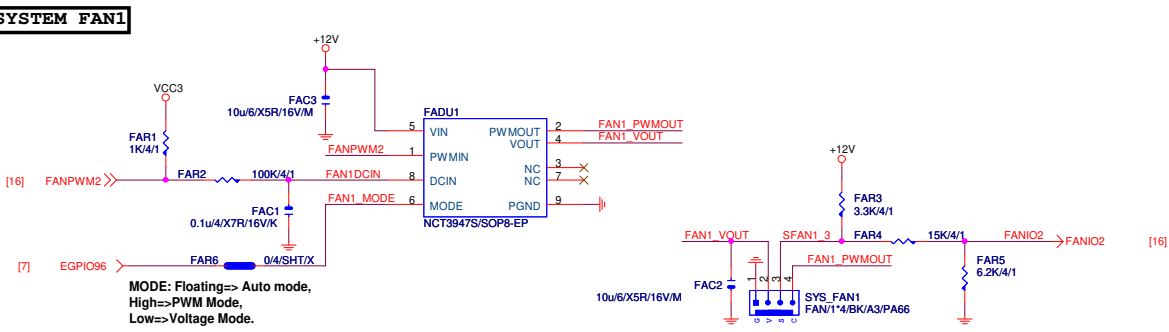




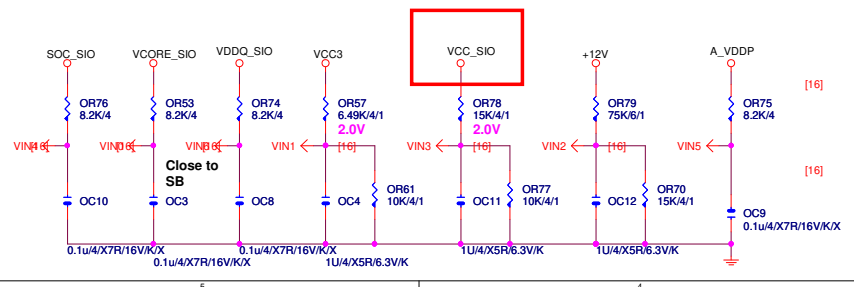
COM PORT



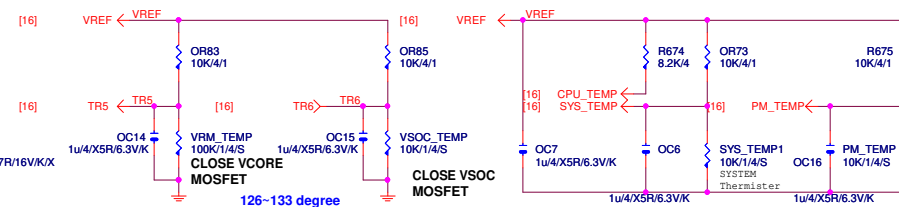
LPT PORT

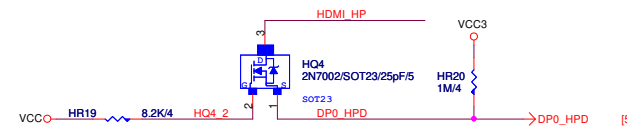
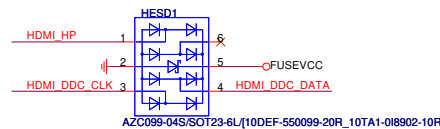
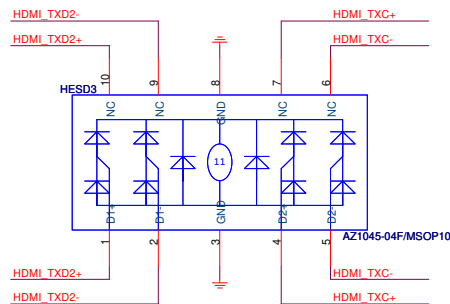
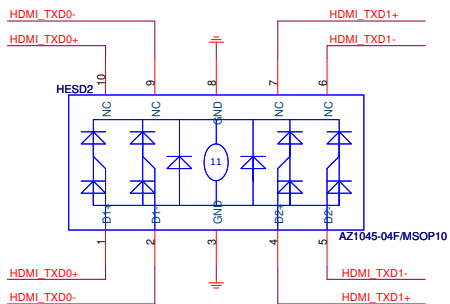
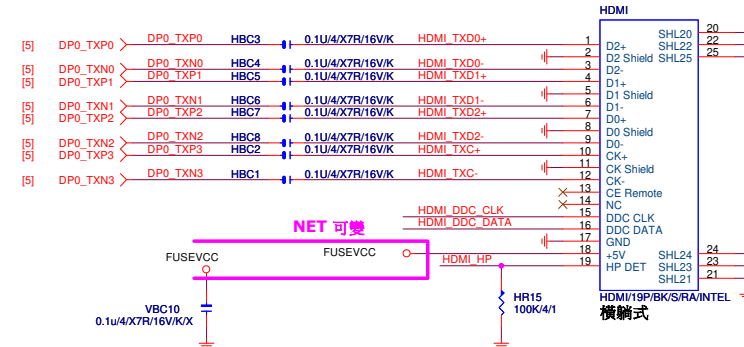
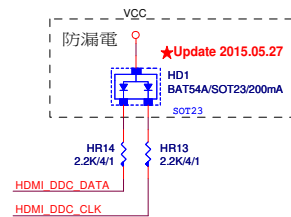
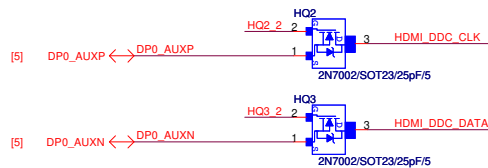
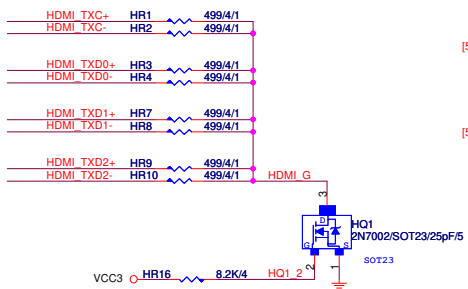


Rev:0.6



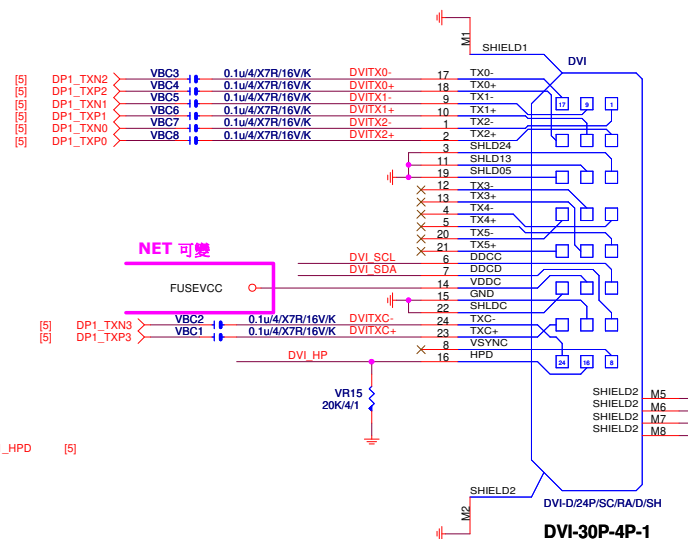
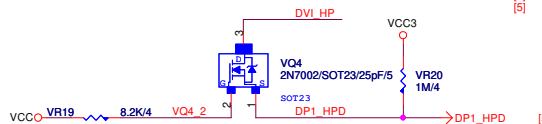
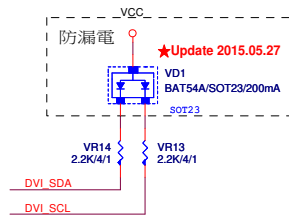
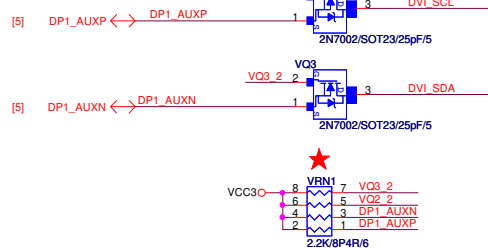
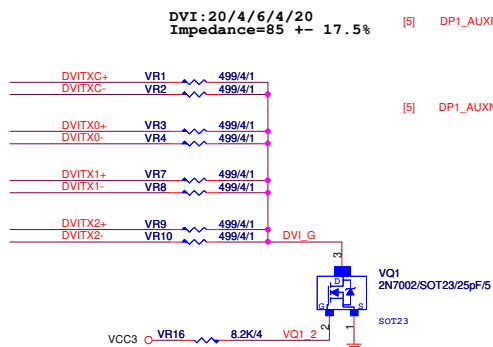
Hardware Monitor circuits - Temperature



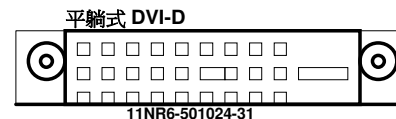
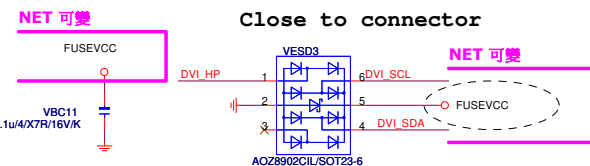
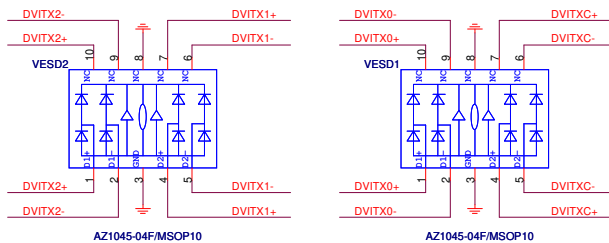


DVI CONN

DVI: 20/4/6/4/20
Impedance=85 +- 17.5%



Close to connector



GIGABYTE

Title: **HDMI,DVI**

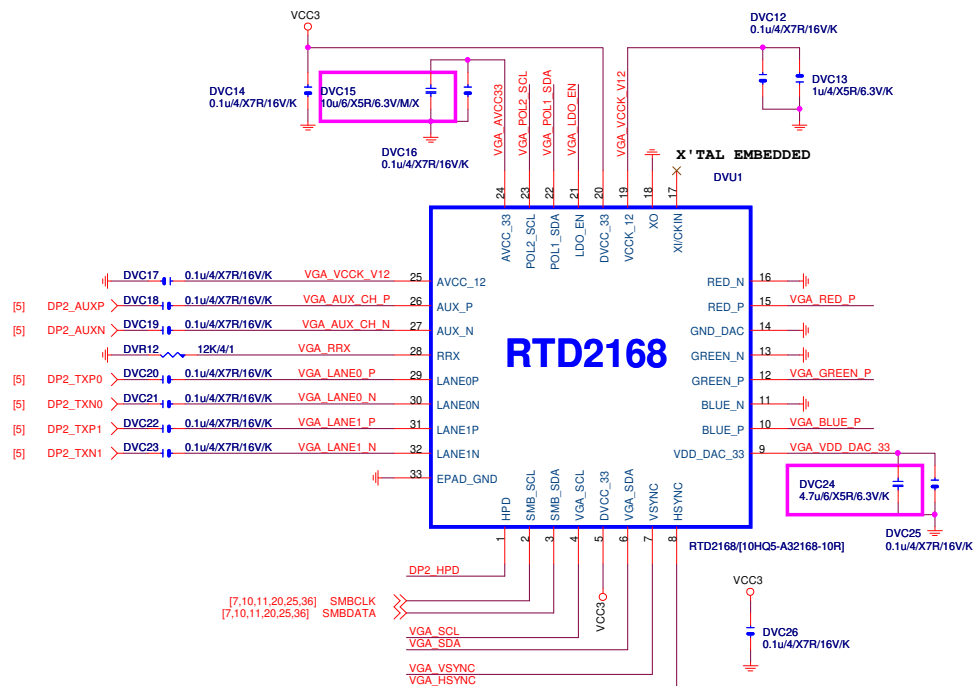
Size: Custom

Document Number: **A520M S2H**

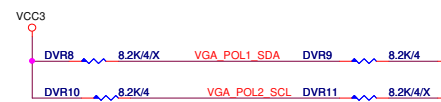
Date: Tuesday, August 04, 2020

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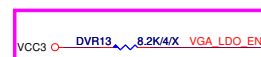


Power on latch



		POL1_SDA(PIN22)	
		0	1
POL2_SCL (PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

Embedded LDO

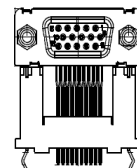
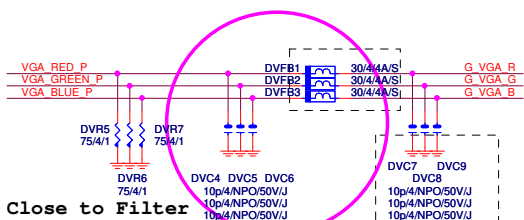
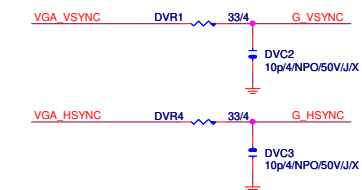


LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

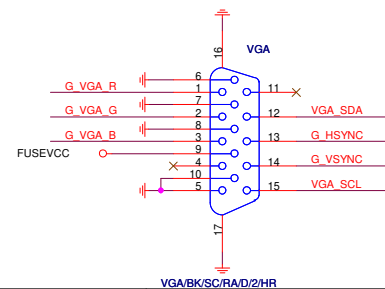
DP HPD



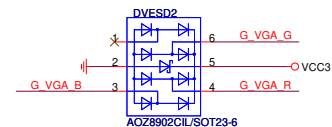
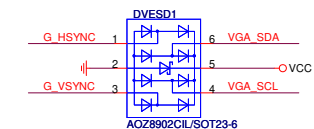
Gigabyte Technology



架高型VGA (BLACK)
Footprint : VGACONN-DH-2



VGA ESD



VGA/BK/SC/RAD/2/HR

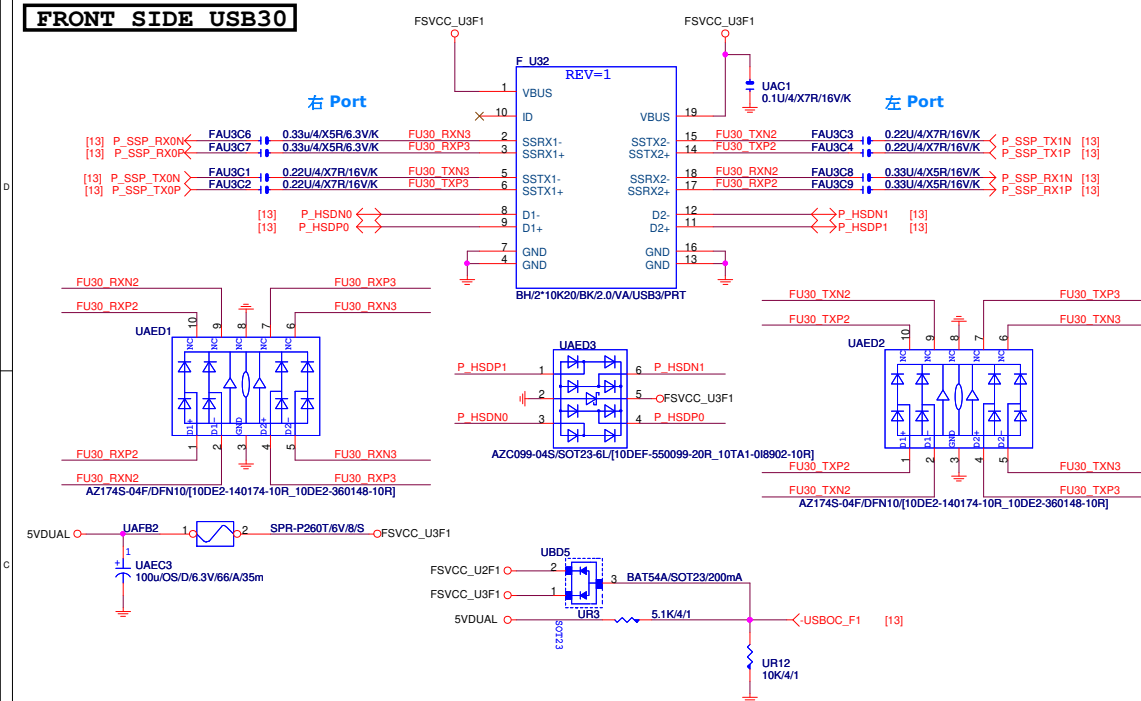
FUSEVCC

DVC1
0.1u/4/X7R/16V/K

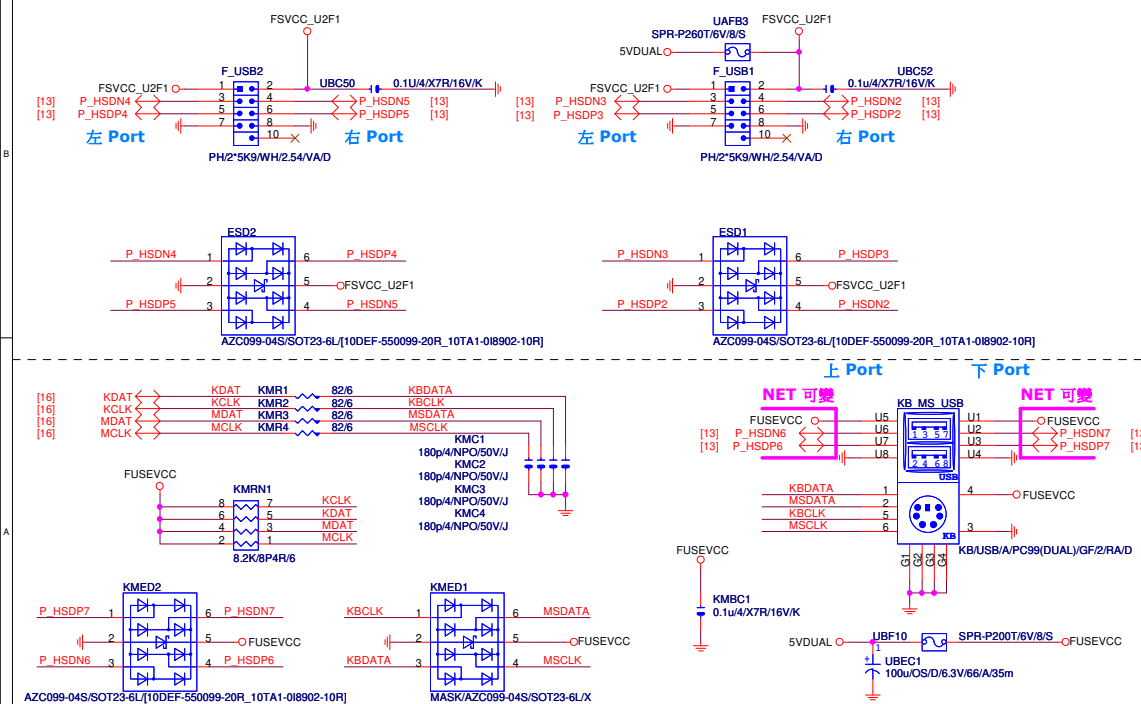
GIGABYTE

Title			
VGA			
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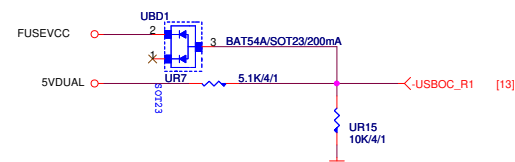
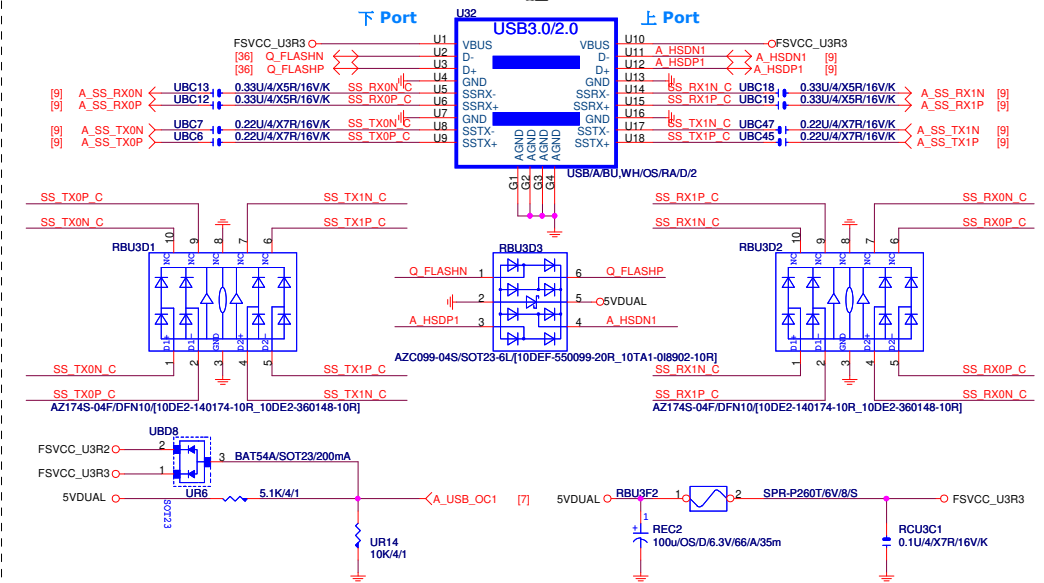
FRONT SIDE USB30



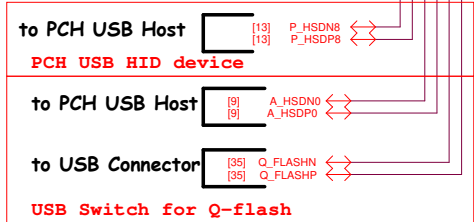
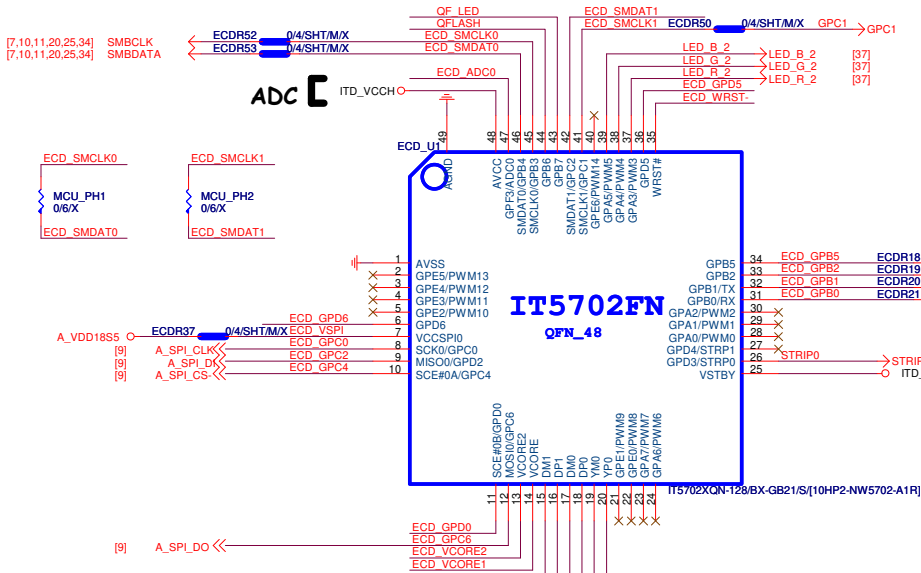
FRONT SIDE USB2.0



FROM CPU WITH Q_FALSH

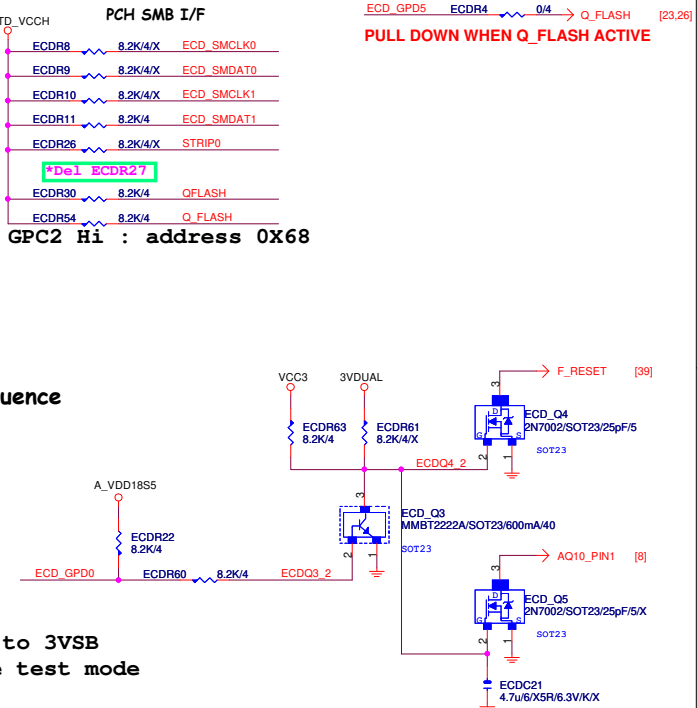


ECD_U1 請放在PCH到BIOS路徑上. 避免線過長



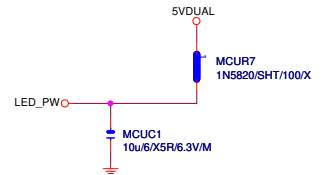
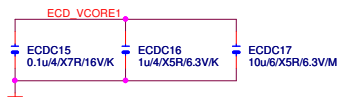
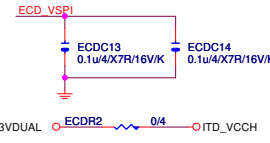
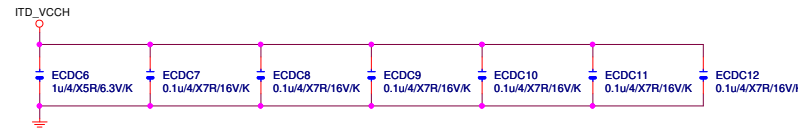
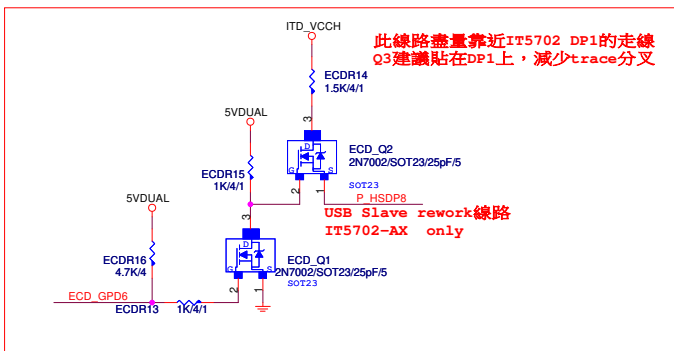
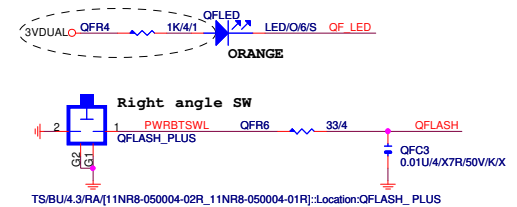
DEMO MODE

Q-Flash Power Sequence



GPD0 pull-up to 3VSB
To ignore the test mode

Q_FLASH BUTTON/LED



第三區 LED

第三區 LED CONTROL

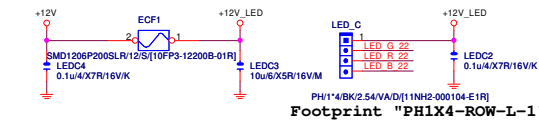
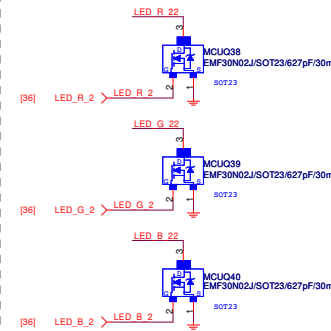
第五區 LED

第二區 LED CONTROL

第五區 LED CONTROL

燈條 LED (LED_C1放在PCB左邊板邊位置)

燈條 LED (LED_C2放在PCB右邊板邊位置)

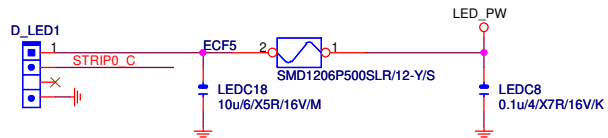


第四區 LED

GIGABYTE™			
File			
CPU/AUDIO/LED_C			
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第六區 LED (靠近左上板邊位置)

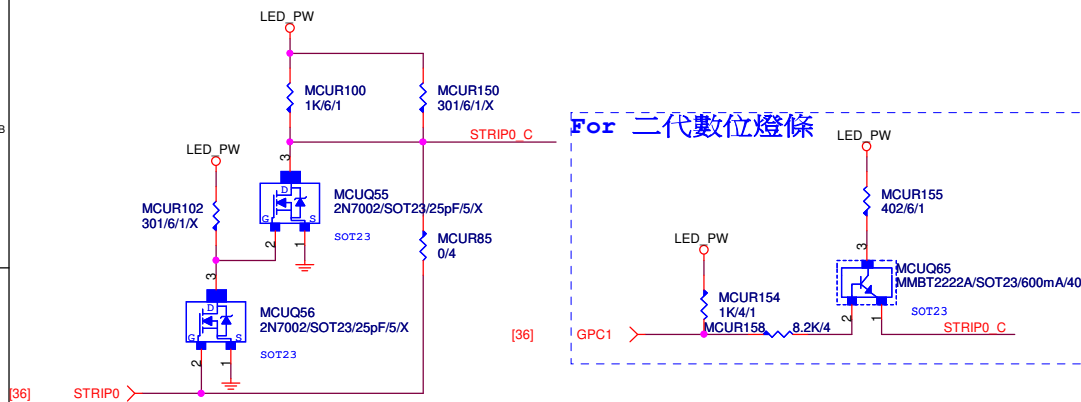
Digital LED Strip1



PH/1*4/BK/2.54/VA/D/[11NH2-000104-G1R]

Footprint PH1X4-CUT3-LED-L

燈條 Level shift



GIGABYTE™

Title

D_LED

Size

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